AN ABSTRACT OF THE DISSERTATION OF

Jifeng Han for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on October 31, 2003.
Title: Novel Power Conditioning Circuits for Piezoelectric Micro Power Generators.

Abstract Approved:

Annette von Jouanne

Advanced low power devices promote the development of micro power generators (MPGs) to replace the batteries to power them. Due to the trend in decreasing integrated circuit (IC) supply voltages, power supply designers are facing more and more serious challenges. The objective of this research is to design a power conditioning circuit (PCC) for use in conjunction with low voltage microelectromechanical systems (MEMS)-based Palouse Piezoelectric Power (P^3) micro heat engine power generation systems. The PCC enables maximum power extraction from a piezoelectric MPG. The proposed PCC includes a rectifier stage and a regulator stage. The rectifier stage is based on the synchronous rectification technique. The dc-dc regulator is a charge pump-based step-down converter. Interleaved discharge (ID) is proposed to reduce the output voltage ripple significantly, without sacrificing the converter efficiency. The proposed step-down charge pump is analyzed with state-space averaging.

In order to facilitate the PSpice simulation of the lead zirconate titanate (PZT) membrane, a simplified PZT model was developed. Both the rectifier and the charge pump are simulated with PSpice. Simulations show that the interleaved discharge

method takes full advantage of the step-down charge pump structure, and provides flexibilities to the design of step-down charge pumps. The designed 200mW 5V/1.2V charge pump has an efficiency of 92.2%, with reduced output ripple. Proof-of-concept demonstration of the proposed PCC includes a 4-stage completely passive charge pump driving an analog wristwatch, proving proper operation of the entire P^3 micro power system.

A maximum output power of 18.8μW has been extracted from a single piezoelectric MPG, with 92% efficiency in the rectifier stage. Arbitrary waveform generator representation (AWGR) of the piezoelectric membrane is also presented. AWGR facilitates ongoing tests and demonstrates the feasibility of cascading many MPGs to extract additional power.

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
31 OCT 2003		**00-00-2003 to 00-00-2003**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Novel Power Conditioning Circuits for Piezoelectric Micro Power Generators	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)	8. PERFORMING ORGANIZATION REPORT NUMBER
Oregon State University,School of Electrical Engineering and Computer Science,1148 Kelley Engineering Center,Corvallis,OR,97331-5501	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

Advanced low power devices promote the development of micro power generators (MPGs) to replace the batteries to power them. Due to the trend in decreasing integrated circuit (IC) supply voltages, power supply designers are facing more and more serious challenges. The objective of this research is to design a power conditioning circuit (PCC) for use in conjunction with low voltage microelectromechanical systems (MEMS)-based Palouse Piezoelectric Power (P3) micro heat engine power generation systems. The PCC enables maximum power extraction from a piezoelectric MPG. The proposed PCC includes a rectifier stage and a regulator stage. The rectifier stage is based on the synchronous rectification technique. The dc-dc regulator is a charge pump-based step-down converter. Interleaved discharge (ID) is proposed to reduce the output voltage ripple significantly, without sacrificing the converter efficiency. The proposed step-down charge pump is analyzed with state-space averaging. In order to facilitate the PSpice simulation of the lead zirconate titanate (PZT) membrane, a simplified PZT model was developed. Both the rectifier and the charge pump are simulated with PSpice. Simulations show that the interleaved discharge method takes full advantage of the step-down charge pump structure, and provides flexibilities to the design of step-down charge pumps. The designed 200mW 5V/1.2V charge pump has an efficiency of 92.2%, with reduced output ripple. Proof-of-concept demonstration of the proposed PCC includes a 4-stage completely passive charge pump driving an analog wristwatch, proving proper operation of the entire P3 micro power system. A maximum output power of 18.8mW has been extracted from a single piezoelectric MPG, with 92% efficiency in the rectifier stage. Arbitrary waveform generator representation (AWGR) of the piezoelectric membrane is also presented. AWGR facilitates ongoing tests and demonstrates the feasibility of cascading many MPGs to extract additional power.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT **unclassified**	b. ABSTRACT **unclassified**	c. THIS PAGE **unclassified**	**Same as Report (SAR)**	**152**	

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std Z39-18

Novel Power Conditioning Circuits for Piezoelectric Micro Power Generators

by
Jifeng Han

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented October 31, 2003
Commencement June 2004

Doctor of Philosophy dissertation of Jifeng Han presented on October 31, 2003.

APPROVED:

_____

Major Professor, representing Electrical and Computer Engineering

_____

Director of School of Electrical Engineering and Computer Science

_____

Dean of the Graduate School

I understand that my dissertation will become one part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

_____

Jifeng Han, Author

ACKNOWLEDGEMENTS

I would like to express my special gratitude and thanks to my advisor, Dr. Annette von Jouanne, for her consistent guidance and support throughout the years of my doctoral study at Oregon State University (OSU). I want to thank her for preparing me extremely well for my future career. I am also very thankful to her for providing with me opportunities to attend such important conferences as IEEE Industry Applications Society (IAS) Annual Meeting, IEEE Power Electronics Specialists Conference (PESC), and Applied Power Electronics Conference and Exposition (APEC).

I would like to express my sincere appreciation to Dr. Thomas G. Dietterich, Dr. Karti Mayaram, Dr. Huaping Liu, and Dr. Alan K. Wallace for being my committee members and for their valuable guidance during my study. I want to thank Dr. Alan K. Wallace for the energy-systems-related knowledge I have learned from his classes.

I would like to thank the Defense Advanced Research Projects Agency (DARPA) for providing financial support for this project. I want to thank Dr. Terri S. Fiez for leading the research team at OSU on the DARPA project, and I want to express my deep appreciation to her and Dr. Karti Mayaram for their valuable advice. I am grateful to Dr. Chenggang Xu and Triet Le for having worked with me as a great team. I would like to express my thanks to Dr. Bob Richards, Dr. Cecilia Richards, Dr. David Bahr, and Jack Skinner at Washington State University for their help and cooperation on the project. My gratitude also goes to Dr. John F. Wager for allowing us use the facility in his labs, and Jeff Bender for providing me with deionized (DI) water.

I am indebted to Shaoan Dai, Andre Ramme, Xiaolin Zhou and other energy system group colleagues for their unselfish help, encouragement, and friendship. It is my pleasure to have been working with such a great team.

I would like to thank my parents, Wenkui Han and Guiyun Han, my parents-in-law, Shufu Chen and Zhengzhi Shao, and my relations and friends for their everlasting support and encouragement during my study. Finally, I would like to express my special thanks to my wife, Haiying Chen, and my son, Qiyu Han, for accompanying me and bringing me good luck. Without their support, devotion, and encouragement, I doubt that I would ever be able to complete my endeavor of pursuing a doctoral degree.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

LIST OF APPENDICES

NOVEL POWER CONDITIONING CIRCUITS FOR PIEZOELECTRIC MICRO POWER GENERATORS

1 INTRODUCTION

1.1 Background

In 1965, Gordon Moore predicted that the number of transistors per integrated circuit (IC) would double every couple of years. This is the very famous Moore's Law. In fact, the evolution of microelectronics technology has followed Moore's Law fairly well for several decades. The appearance of wearable electronic devices, such as electronic wristwatches, mobile telephones, hearing aids, implanted cardiac pacemakers, and personal digital assistants (PDAs) among others, has transformed the way people live. Wireless integrated network sensors (WINS) are widely used in civil and military applications. Advances in IC technology, following Moore's Law, have enabled the reduction of the size/weight and energy requirement of these devices. For example, by 2005, the power consumption of the Bluetooth communication technique will drop from 12.5mW (in 1998) to 5.1mW [1]. The power supply voltages for ICs are being continuously reduced in order to increase the integration densities, reduce the power consumption, and increase the reliability of gate dielectrics [2].

In digital electronics, the power consumed to charge and discharge a load capacitance C_L can be expressed in terms of switching frequency f, load capacitance and supply voltage V_{dd} as follows [3]

$$P_c = fC_L V_{dd}^2 \tag{1-1}$$

From (1-1), it can be clearly seen that decreasing the supply voltage can reduce the power consumption quadratically. According to the "International Technology

Roadmap for Semiconductors, 2002 update" [2], by the year 2016, the supply voltage for high-performance logic technology will drop to 0.4V.

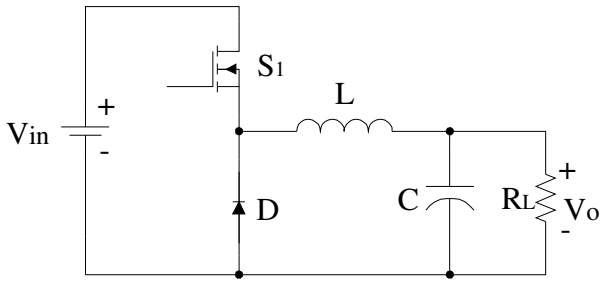
With the continuous drop in IC supply voltages, power supply designers are facing more and more serious challenges, such as efficiency, response time, output ripple, size/weight, cost, etc. Because the output voltage of the power supply is so low, any voltage drop on any devices in the power supply may lead to significant efficiency degradation. For instance, diodes are commonly used in power supplies. The typical forward voltage drop of a silicon diode is around 0.7V, and even a good Schottky diode may have a typical forward voltage drop of 0.3V. It is obvious that this kind of voltage drop is intolerable for a power supply whose output voltage is only 0.4V, as the diodes will constitute the biggest part of power loss.

Fig. 1.1 (a) illustrates a conventional buck (step-down) dc-dc converter. Power supply designers have been struggling very hard to design high-efficiency power supplies. In low-output-voltage switch-mode power supplies (SMPSs), synchronous rectification (SR) has already been widely applied to improve power supply efficiency [4]. Fig. 1.1 (b) shows the application of SR in a buck dc-dc converter. Fig. 1.1 (b) is the same as Fig. 1.1 (a) except that the freewheeling diode D is replaced with a power switch, S_2. Since the on-resistance of the power switch may be very low, the efficiency of the converter is improved.

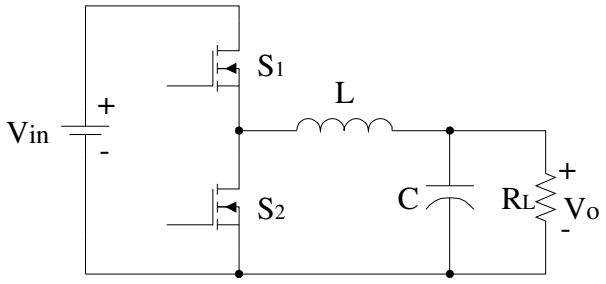
Usually, low-power electronic devices are battery powered. Whether the batteries are rechargeable (secondary) or non-rechargeable (primary), they all suffer from the same drawbacks: bulky size, limited service life, and difficult or impractical replacement in applications such as unattended sensors or implanted cardiac pacemakers.

An attractive alternative to batteries is micro power generators (MPGs), which have recently gained increased attention. An MPG is expected to be five-to-ten times smaller than a comparable battery [5], and features enhanced performance. Some

MPGs can scavenge attainable energy from the environment of the system and convert it into useful electrical energy [6]-[8]. Possible "fuel-free" environmental energy sources for MPGs include human body/activities, ambient mechanical vibrations, acoustic energy, waste heat from IC chips, solar energy, and so on. There are also other "non-fuel-free" energy sources, such as natural gas, biomass, nuclear energy, etc. Fig. 1.2 shows the system schematic of an MPG. The MPG extracts energy from the environment, and generates an ac output voltage, which must be converted to the required regulated voltage with a power conditioning circuit (PCC). The output power of the PCC may be stored for pulse power requirements. Meanwhile, if the loads only require limited continuous power, it can be provided directly by the PCC.



(a) Conventional buck converter



(b) Synchronous buck converter

Fig. 1.1. Buck dc-dc converter.

In 1988, the first kinetic energy watch in the world appeared [9]. The MPG in this watch converts mechanical energy (arm movement) to electrical energy with an oscillating weight, a gear train, and a small motor.

Piezoelectric materials, such as lead zirconate titanate (PZT), and polyvinyldifluoride (PVDF), create electrical charge when mechanically strained. This property is termed piezoelectricity, which was discovered in 1880 by Pierre and Jacques Curie. When placed in an electric field, piezoelectric materials become strained. The PVDF material is more flexible than PZT and suitable for high-pressure operation, and the output voltage is high. On the other hand, the PZT material is more suitable for high-temperature operation, and its output voltage is lower compared with that of the PVDF material. Piezoelectric materials are commonly used in piezo sensors (generators) and piezo actuators (motors). Piezo sensors convert mechanical energy to electrical energy, and piezo actuators convert electrical energy to mechanical energy.

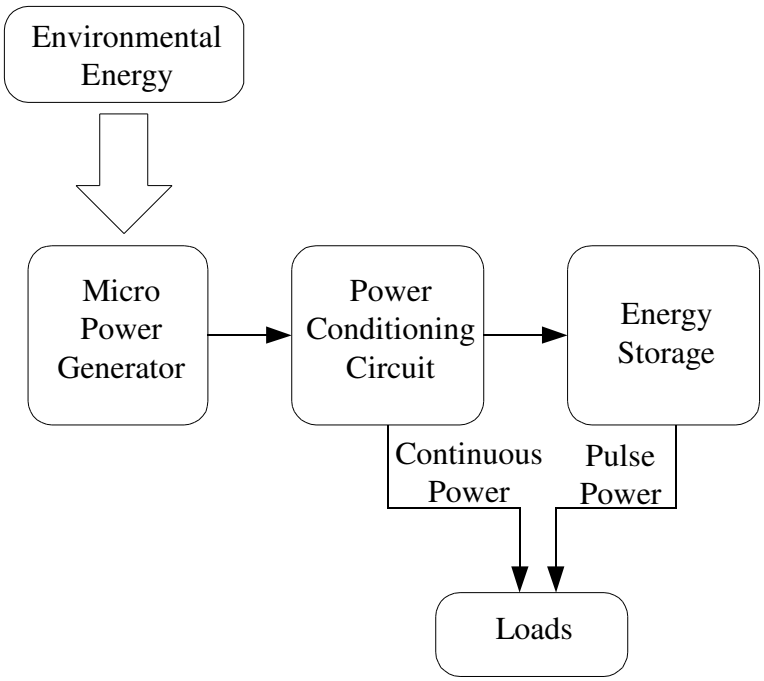


Fig. 1.2. Schematic of an MPG system.

The use of a thin PZT film/plate for a micro power supply, as shown schematically in Fig. 1.3, is a new and exciting application [10]-[12]. In this application, the piezoelectric laminate is mechanically forced to vibrate and thus, it works as a generator to transform the mechanical energy into electrical energy. Together with an appropriately designed power conditioning system, this piezoelectric generator has great potential to be used as a micro power supply for microelectronic and micro-electromechanical systems (MEMS) devices.

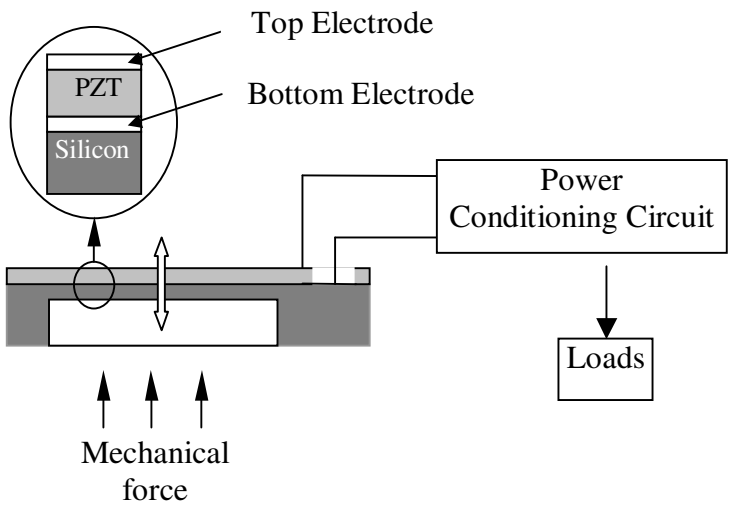


Fig. 1.3. Block diagram of the piezoelectric power generator.

Researchers at Washington State University have proposed a MEMS-based P^3 micro heat engine power generation system [13]. Fig. 1.4 shows a unit cell of such an MPG. The unit cell consists of a cavity filled with a working fluid, which is a mixture of liquid and vapor. It can be seen that there is a vapor bubble in the cavity. The bottom of the cavity is sealed by a thin-film piezoelectric membrane, which serves as the power generator. When heat is conducted in, the working liquid evaporates, causing the piezoelectric membrane to flex outward. The strained piezoelectric membrane then generates useful electrical energy. When heat is conducted out, the vapor condenses, causing the piezoelectric membrane to flex inward. Due to

modularized design, many unit cells could be conveniently connected in series or in parallel to obtain the required voltage and power. Fig. 1.5 shows such a system [14]. A single P^3 micro heat engine is expected to provide 1mW of continuous power with a power density of ~1W/cm^3 and energy density of ~1000Whr/kg.

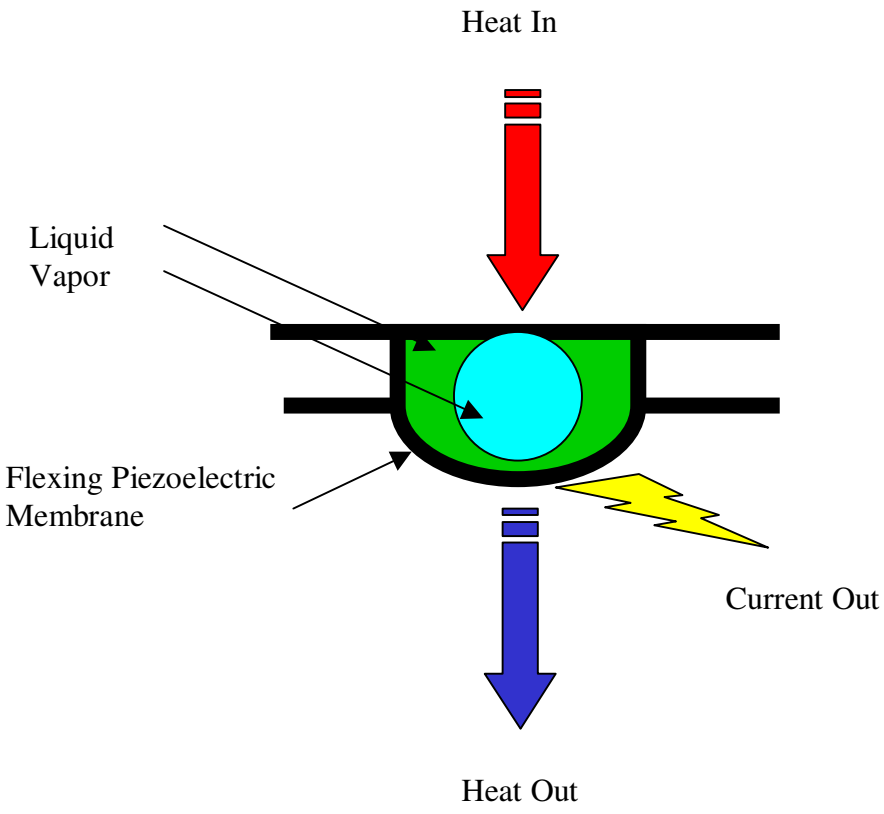


Fig. 1.4. Schematic of a unit cell of the P^3 micro heat engine power generator [13].

To obtain regulated dc voltages required by electronic loads, we can employ one of the three general types of dc-dc converters: linear regulators, switch-mode power converters, and charge pumps (also known as switched-capacitor dc-dc converters).

The block diagram of a linear regulator is illustrated in Fig. 1.6. In this circuit, the transistor acts as an adjustable resistor. The voltage difference between the input and

the output, i.e., $V_{in} - V_0$, appears across the transistor and causes power losses in it. The efficiency of a linear regulator is low unless the required output voltage is slightly below the input voltage. In order for the power supply to work, the minimum input voltage $V_{in,\min}$ should always be higher than the output voltage V_o.

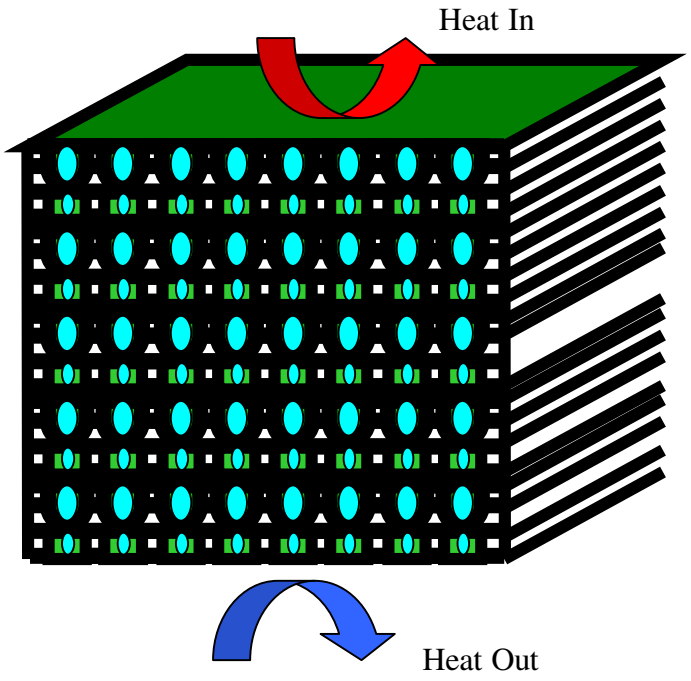


Fig. 1.5. Schematic of the P^3 micro heat engine power generator [14].

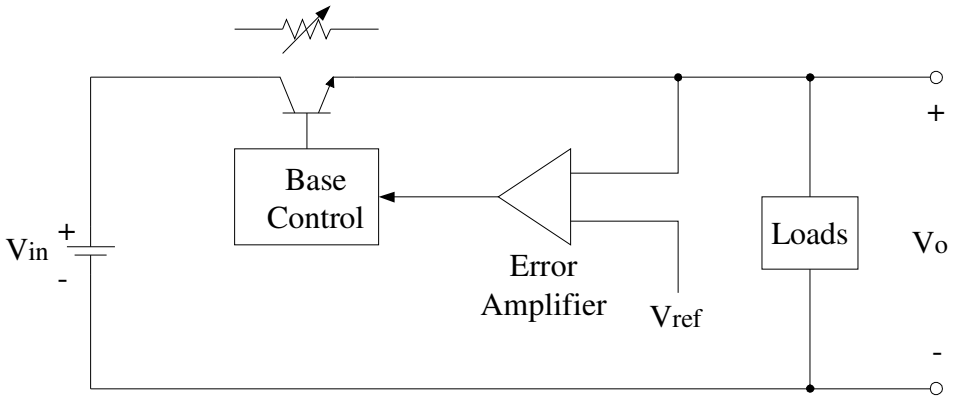


Fig. 1.6. Block diagram of a linear regulator.

Switch-mode power converters are controlled by pulse-width modulation (PWM). Fig. 1.7 shows a PWM switch-mode dc-dc converter. A switch-mode power converter can be classified into three categories: buck (step-down), boost (step-up), and buck-boost (step-down/step-up). A buck converter has already been shown in Fig. 1.1. For switch-mode converters, it is theoretically possible to obtain 100% efficiency, if the parasitic effects are zero.

The disadvantage of switch-mode power converters is that they need magnetic devices, e.g., inductors and/or transformers, which are key components for controlled transfer of energy. Even if the switching frequency is very high, magnetic devices are still unavoidable, which makes it hard to design low-profile high-density power supplies. Both conventional (wire wound) and planar magnetic devices are bulky due to the use of magnetic cores. Conventional wire wound inductors and transformers are not amenable to mass production, thus increasing the manufacturing cost of power supplies. Planar magnetic devices can either be constructed as stand alone components, with a small multilayer printed circuit board (PCB), or integrated into a multilayer PCB of the power supply [15]. They feature relatively low profile, excellent thermal characteristics, low leakage inductance, and excellent repeatability of properties. However, it is currently impractical to integrate planar magnetic devices on-chip due to their high surface to volume ratio. Although on-chip inductors/transformers are available in standard IC processes, it has been found that the quality factor (Q, impedance to resistance ratio) is poor [16]. These on-chip inductors/transformers are used in radio frequency (RF) circuits, but they are unsuitable in high-efficiency power supplies.

A third category of dc-dc converters, charge pumps, has gained increased attention recently. They rely solely on switches and capacitors for energy transfer. By manipulating the turn-on and turn-off times of the switches, the converter undergoes several different states, thus controlling the charging and discharging trajectory of the capacitors, and obtaining the required output voltage. High quality on-chip capacitors are easier and more efficient to fabricate than high value inductors. Unlike switch-

mode dc-dc converters, charge pumps need not employ magnetic components. Hence, they are inherently amenable to monolithic integration [17]. Fig. 1.8 shows the schematic of a charge pump voltage doubler. Charge pumps are widely used in flash memory circuits [18], liquid crystal display (LCD) drivers [19], filters [20], etc.

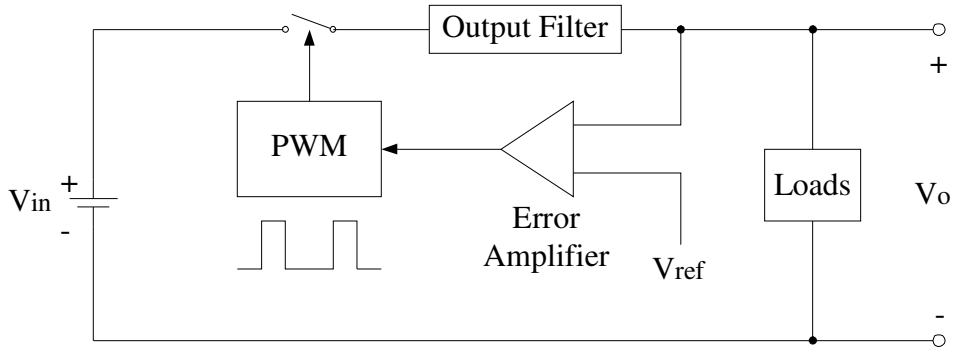


Fig. 1.7. Block diagram of a PWM switch-mode power converter.

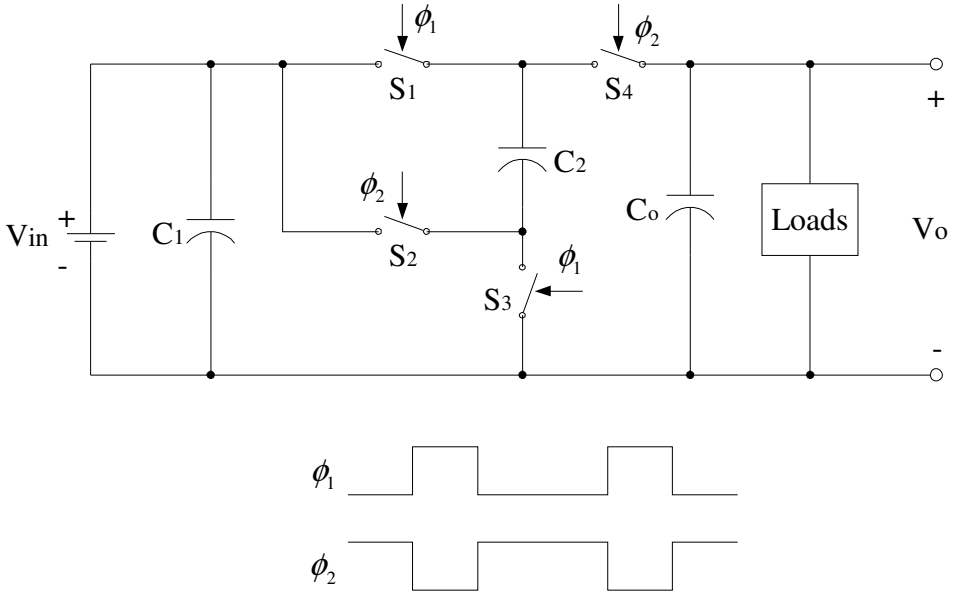


Fig. 1.8. Charge pump voltage doubler.

The circuit structure of a charge pump determines that its efficiency can never reach 100%. For charge pumps, there is an inherent power loss that can never be avoided. This is due to step voltage changes (ΔV) across the capacitor. This energy loss can be shown to be [21]

$$E = \frac{1}{2} C(\Delta V)^2 \tag{1-2}$$

1.2 Previous Work

The feasibility of scavenging energy from human body/activities has been studied [1], [6], [22]. The head is one of the warmest parts of one's body, and the estimated heat power radiation is 15W [22]. It is estimated that at least 500mW of useful electrical power can be harvested from common clothes such as a cap. Therefore, it is possible to feed wearable systems from body heat dissipation via electrothermal conversion. In [6], Shenck and Paradiso demonstrated that when people walk, parasitic power in shoes could be harvested through a PVDF or PZT generator to power a radio frequency tag that transmits a short-range, 12-bit wireless identification code.

Other attainable ambient energy sources include mechanical vibration energy [8], [23], [24], acoustic energy [25], etc. In [8], a system was proposed to convert ambient mechanical vibration into electrical energy, with an approximate net output power of 8μW. The energy is converted through a MEMS variable capacitor. In [24], a moving coil electromagnetic transducer was used to convert vibration energy into electrical energy. The authors claimed that the generated power was on the order of 400μW. The power regulator was a synchronous buck converter, with the two Metal-Oxide-Silicon Field Effect Transistors (MOSFETs) integrated on chip, and the 56μH inductor and the 10μF capacitor were external to the chip. In [25], Horowitz, et al, presented an acoustic energy harvester employing an electromechanical Helmholtz resonator with a PZT generator. A simple linear regulator was adopted to show the feasibility of acoustic energy reclamation. The estimated output power was 7.4mW.

In [26], an adaptive piezoelectric energy harvesting circuit was proposed to harvest maximum power from the vibrating piezoelectric transducer. This is the only published work that has been found to work on maximum power extraction from piezoelectric generators. Fig. 1.9 shows the block diagram of the proposed energy harvesting circuit. The energy harvesting circuit consists of a full bridge diode rectifier and a buck dc-dc converter. At the highest excitation level, the rectified open-circuit voltage was 95.31V, and the harvested power was 70.42mW. The piezo wafer size (inch) is $1.81 \times 1.31 \times 0.010$. An adaptive control technique for the dc-dc converter was used to realize optimal power transfer and maximize the power stored in the battery. The adaptive controller was based on a digital signal processor (DSP).

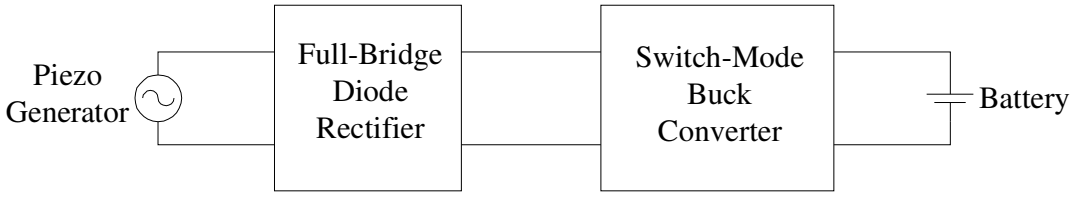


Fig. 1.9. Diode bridge rectifier used in [26].

1.3 Research Objectives

In the previously mentioned P^3 engine, piezoelectric membranes generate an ac voltage. The objective of this research is to design a power conditioning circuit (PCC) for use in conjunction with the MEMS-based P^3 micro heat engine power generation system. The PCC draws useful electric power from the P^3 engine and converts it to the regulated dc voltage. Fig. 1.10 shows the schematic of the P^3 system. The proposed PCC includes two stages: a rectifier as the first stage, and a dc-dc converter as the second stage. It is also desirable to enable maximum power extraction from the P^3 micro heat engine power generator.

So far, little attention has been paid on how to extract maximum power from MPGs. Although an adaptive piezoelectric energy harvesting circuit was proposed to harvest maximum power from the vibrating piezoelectric transducer in [26], the first stage of this circuit is a simple diode bridge rectifier, as already shown in Fig. 1.9. It is unsuitable for low-voltage MPGs whose output voltage is comparable to a diode forward voltage drop. This research has investigated the possible application of a synchronous rectifier as the first stage of the PCC.

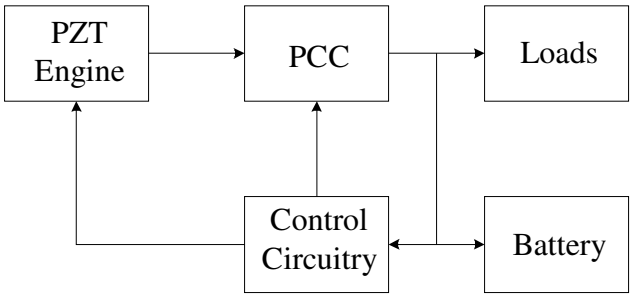


Fig. 1.10. Schematic of the P^3 system.

In an effort to achieve miniaturization, it is desirable to integrate the PCC on a single chip. Conventional dc-dc converters such as buck-boost converters feature high efficiency but they need bulky magnetic components. The charge pump is a promising dc-dc converter in that it is composed of capacitors and MOSFETs, which both can be integrated on chip (with a very limited number of external capacitors that are still too large to implement on an IC with current technology). The fact that the piezoelectric membrane is capacitive also makes a charge pump dc-dc converter more attractive. This work has designed a low-output-ripple charge pump as the second stage of the PCC.

Fig. 1.11 shows the commonly used Van Dyke's model for representing the equivalent circuit of a piezoelectric membrane. L_1, C_1, and R_1 are mass, elastic

compliance and mechanical damping transformed into electrical magnitude by the piezoelectric effect, respectively. C_o is the capacitance in the absence of mechanical deformation at the resonant frequency [27]. The involvement of these mechanical and material parameters makes this model too complicated for PCC designers. From the viewpoint of power extraction, the PZT should work at resonance. Instead of using Van Dyke's model in the simulation, this research has developed a simplified PZT model, which is much easier for PCC designers to manipulate and facilitates the simulation work.

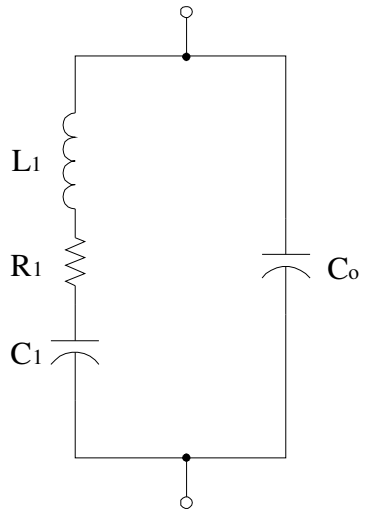


Fig. 1.11. Van Dyke's PZT model.

Since the power level of a single generator cell is very low, in order to achieve higher power, it is necessary to connect many cells in series or in parallel according to the load requirements. Because the respective research at OSU and WSU is being carried out simultaneously, the actual micro P^3 heat engine is unavailable to OSU while it is being used by the Mechanical Engineers at WSU. Thus, researchers at WSU have developed a bulge tester, which is used to simulate the action of the micro heat engine that drives the PZT membranes [28]. Under these circumstances, it is impractical to build several bulge testers for PCC experiments. An alternative to the bulge tester is to develop a representative system with an arbitrary waveform

generator and the necessary interfacing circuits. The work has developed an arbitrary waveform generator representation (AWGR) system that can replace the bulge tester and the PZT membrane for some ongoing experiments.

1.4 Dissertation Organization

This dissertation is organized in the following way. Chapter 1 provides a brief introduction to the background information of the research, previous related works, and the research objectives. In Chapter 2, a novel power conditioning circuit for micro power generators is designed. The rectifier stage and the dc-dc regulator stage are designed separately. Three possible topologies of the rectifier are presented. The proposed rectifier stage is based on the synchronous rectification technique. The dc-dc regulator is a charge pump-based step-down converter. Interleaved discharge (ID) is proposed to reduce the output voltage ripple greatly, without sacrificing the converter efficiency. The proposed step-down charge pump is analyzed with state-space averaging. The superiority of the proposed ID method will be verified by simulation.

In Chapter 3, the proposed PCC is verified by PSpice simulation. A simplified PZT model that is PCC designer friendly is developed. The three schemes of the rectifier stage are simulated and compared. A 200mW, 5V/1.2V, with less than 1% ripple step-down charge pump is designed and simulated. The advantages of the proposed ID method are given.

The experimental setups of the proof-of-concept demonstration and the bulge tester are presented in Chapter 4. In Chapter 5, the experimental results and discussions are presented. Arbitrary waveform generator representation (AWGR) of the PZT membrane is presented in Chapter 6. Finally, Chapter 7 concludes the dissertation and provides suggestions for future work.

2 DESIGN OF THE POWER CONDITIONING CIRCUIT

2.1 Introduction

Considering the fact that the MPG generates an ac output and the load needs a regulated dc voltage, we can imagine that a power conditioning circuit (PCC) that connects the MPG and the load is necessary. The PCC includes two stages: an ac-dc rectifier stage and a dc-dc regulator stage. The two stages are connected by a dc link capacitor. Fig. 2.1 illustrates the schematic of the PCC. The ac-dc rectifier converts the ac output from the MPG into an unregulated dc voltage. Usually, this stage consists of a diode rectifier.

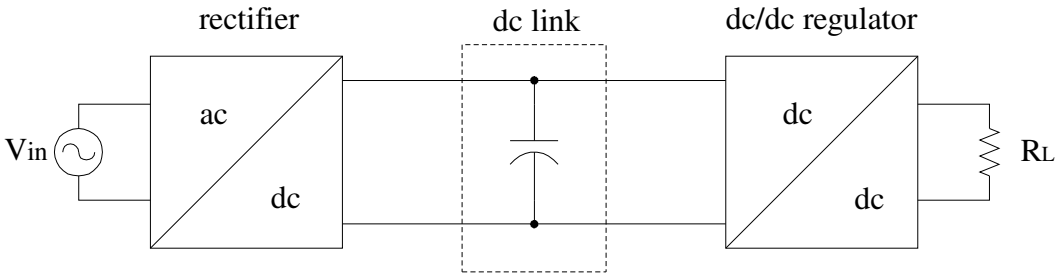


Fig.2.1. Schematic of the power conditioning circuit.

By means of the dc link, the output and input can be decoupled, e.g., the design of the dc-dc regulator is independent of the ac side variation. Therefore, the dc link capacitor is a necessity. The same technique has been used in adjustable speed drives (ASDs) [29].

As already discussed in Chapter 1, there are mainly three topologies for the dc-dc regulator: linear regulator, switch-mode regulator, and charge pump. Because of the advantages that the charge pump only requires switches and capacitors and the PZT

membrane itself is capacitive, this work will only consider a charge pump-based dc-dc regulator topology.

Because the research on the micro heat engines is still in progress at Washington State University, there exists some uncertainty in the dc link voltage level, i.e., the required step-down ratio of the charge pump is unknown. As such, this work will investigate a generic step-down charge pump. It is well known that high voltage is more suitable for efficient power transmission. This also holds for computer applications: the voltage delivered to the motherboard is usually higher than the load-required supply voltages. For some low-voltage applications, a step-down dc-dc regulator might be indispensable.

Nowadays, computers need several supply voltages. In switch-mode power supplies (SMPSs), the percentage output voltage ripple is usually specified to be less than 1% [4]. Table 2.1 shows some typical ripple specifications for different supply voltages [30].

Table 2.1 Ripple specifications for computer power supplies [30].

Output DC Voltage (V)	Maximum Ripple (mVpp)
+12	120
+5	50
+3.3	50
-5	100
-12	120
+5 standby	50

Table 2.2 is derived from the "International Technology Roadmap for Semiconductors, 2002 update". According to this roadmap, the power supply voltage will drop to 0.4V by 2016. This presents serious challenges for power supply designers. If the required voltage ripple is still 1%, then its peak-to-peak ripple will be less than 4mV by 2016.

Table 2.2 International technology roadmap for semiconductors, 2002 update [2].

	2002	2005	2007	2010	2013	2016
Power Supply Voltage (V) (High performance)	1.0	0.9	0.7	0.6	0.5	0.4
Power Supply Voltage (V) (Low operating power, high V_{dd} transistors)	1.2	1.0	0.9	0.8	0.7	0.6
Allowable Max. Power (W) (High performance with heatsink)	140	170	190	218	251	288
Chip Frequency (MHz)	2317	5173	6739	11511	19348	28751

There are some approaches to reducing the power supply output voltage ripple. For example, we can increase the capacitance value of the output filter. Although this approach is very easy, it may not meet low-cost, high-power density design requirements.

Recently, there have been numerous investigations on the so-called interleaving technique in switch-mode power supplies [31]-[34], as shown in Fig. 2.2. The N converter cells are physically paralleled and are operated at the same switching frequency, but are phase-shifted by $2\pi/N$ with respect to one another. By interleaving N-paralleled converter cells, the input/output ripple can be reduced by 1/N or more. Employing interleaving techniques can also improve the power level of the power supply. Interleaving techniques have also been used to reduce output ripple in charge

pumps [35], [36]. The shortcoming of the conventional interleaving technique is increased component count and complicated control.

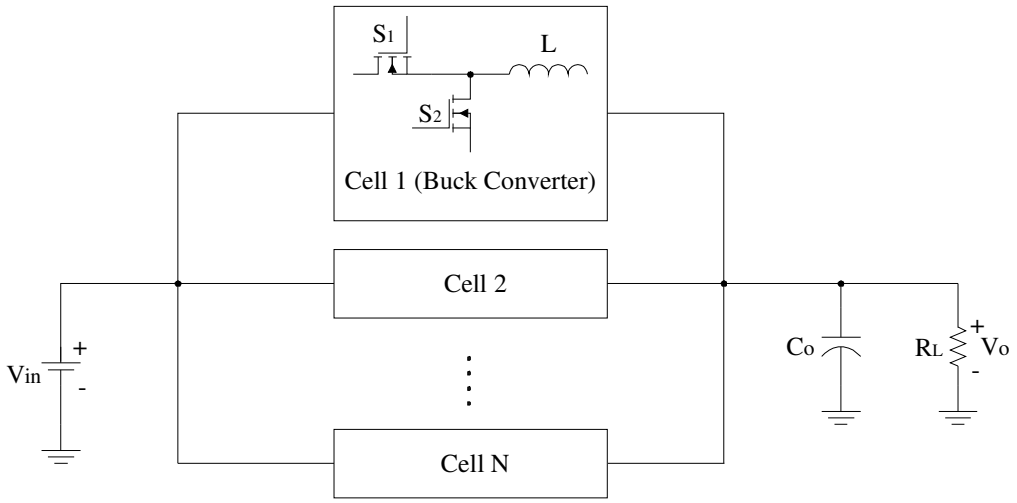


Fig. 2.2. Interleaving technique.

Step-down charge pumps have a structure that can potentially be utilized to reduce the output voltage ripple, without resorting to the above ripple-reduction approaches. This work will propose a new control strategy that will reduce the voltage ripple greatly.

2.2 Rectifier Stage

At the current stage of the DARPA project, 21-layer lead zirconate titanate (PZT) membranes have been adopted as the piezoelectric generator. The peak-peak output voltage of a single PZT membrane is in the range of 1.8~2.5V_{PP}. In this case, the diode rectifier's forward-voltage drop constitutes a significant fraction of the PZT output voltage. Even the commonly used Schottky diodes still have a relatively large voltage drop. Therefore, rectification is a nontrivial issue.

2.2.1 Scheme I: Diode-Resistor Pair Rectifier

Fig. 2.3 shows scheme I of the rectifier stage. As it can be seen, there is a diode, which acts as a single-phase half-wave rectifier. The resistor R_c is used to increase the output power of the circuit. It has been found that without this resistor, the output power is almost zero. After adding R_c, the output power is greatly increased. For the PZT membranes used, it has been found that R_c in the range from 40kΩ~60kΩ can help extract more power. In Chapter 3, we will develop a modified PZT model, and the function of R_c will be explained there.

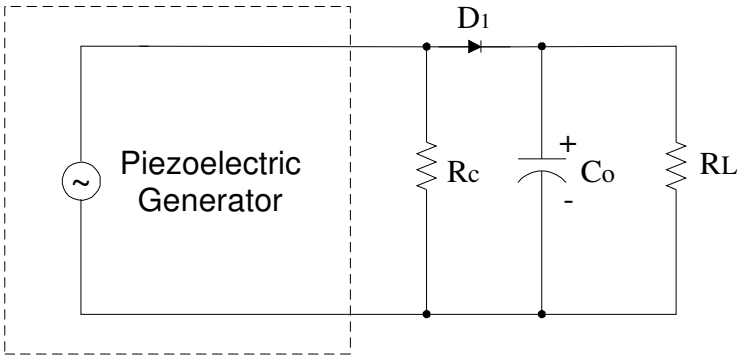


Fig. 2.3. Scheme I of the rectifier circuit.

2.2.2 Scheme II: Diode-Diode Pair Rectifier

Fig. 2.4 shows a very famous ac-dc voltage doubler [37], [38]. This capacitor-diode network has the capability to convert an ac input voltage $V_{in} = E\sin(\omega t)$ into a dc output voltage $V_{C0} = 2E$. During the negative half cycle of the input sine wave, capacitor C_1 is charged to $V_{C1} = E$ through diode D_2. Then, when the positive half cycle of V_{in} comes, the voltage of C_1 and V_{in} will stack together, and through diode

D_1, C_0 is charged to a dc voltage of approximately $V_{C0} = 2E$, if the load current is not too high. Voltage multipliers based on this technique have been extensively used in televisions.

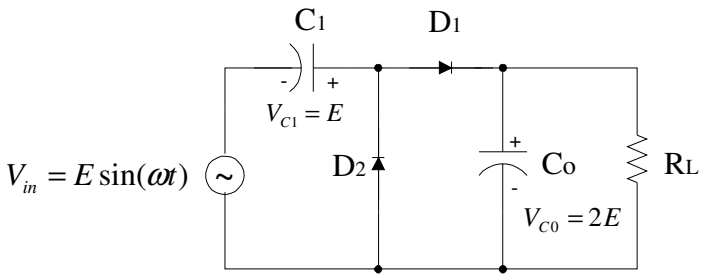


Fig. 2.4. An ac-dc voltage doubler.

Since the PZT membrane is capacitive, we can utilize the equivalent terminal capacitor of the PZT membrane, and develop a modified ac-dc voltage doubler. This modified ac-dc voltage doubler is dubbed scheme II in this work, as shown in Fig. 2.5. Note that in scheme II the inherent capacitance of the piezoelectric membrane is uncontrollable for PCC designers.

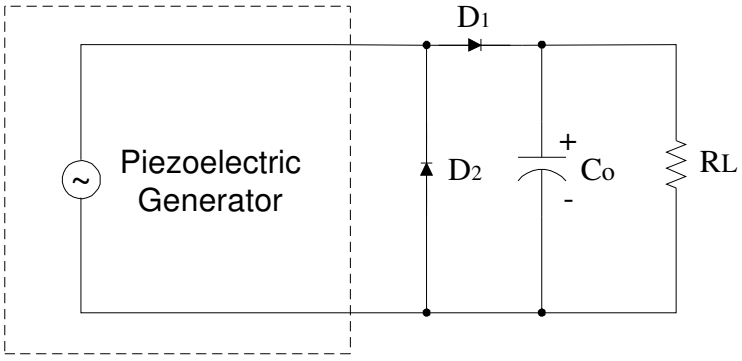


Fig. 2.5. Scheme II of the rectifier circuit.

2.2.3 Scheme III: Synchronous Rectifier

In this work, a synchronous rectifier, as shown in Fig. 2.6, is proposed to improve the PCC efficiency. The comparator senses the source-drain voltage of the N-channel MOSFET. The MOSFET can only work in the third quadrant, i.e., it only conducts when the source of the MOSFET is positive with respect to its drain. The MOSFET body diode would not be forward-biased due to the very low on-state resistance R_{DS} of the MOSFET. When the drain of the MOSFET is positive with respect to its source, the body diode is reverse-biased. Scheme III is based on the SR technique and is expected to further increase the extracted power from the piezoelectric generator.

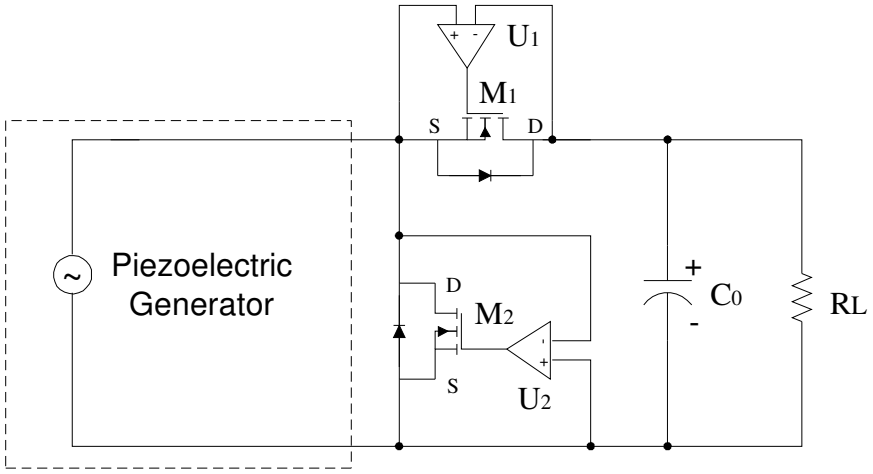


Fig. 2.6. Scheme III: synchronous rectifier.

2.3 Regulator Stage

As mentioned previously, this work will adopt a charge pump as the regulator stage. Charge pumps have been used for many years. Commercial products include LM2781 [36], 7660 voltage inverter [39], etc.

As the allowable maximum power increases, the most suitable computer on-board distribution voltage would be 5V, or even higher, due to the low power loss associated with the power distribution system. Based on the state-of-the-art power supply distribution technology, projections of the IC development, and the characteristics of this work, a generic charge pump will be designed, aiming at a 5V/1.2V step-down ratio and a ripple of less than 1%. The power is chosen to be 200mW since the task of this work is to operate in the DARPA project low power range. 200mW of power is enough for integrated circuits such as operational amplifiers, unattended sensors, etc.

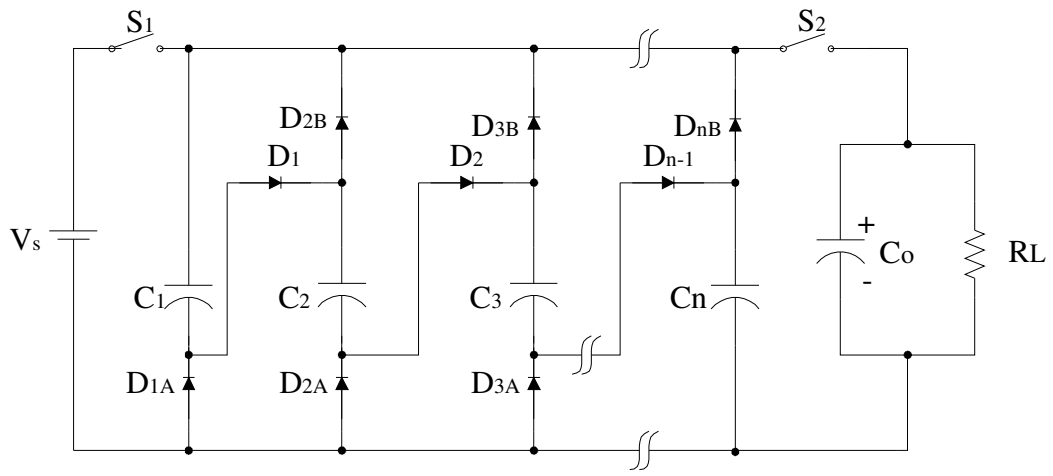


Fig. 2.7. Conventional n-stage step-down charge pump.

2.3.1 Conventional Step-Down Charge Pump

Fig. 2.7 shows the schematic of a conventional n-stage step-down charge pump. Fig. 2.8 illustrates the timing diagram and some typical waveforms. During the charging interval, capacitors C_1~C_n are charged in series. During the discharging interval, the capacitors are connected in parallel so that they can discharge

simultaneously. The circuit topologies of the two states are shown in Fig. 2.9. The output voltage is ideally

$$V_o = \frac{V_s}{n} \tag{2-1}$$

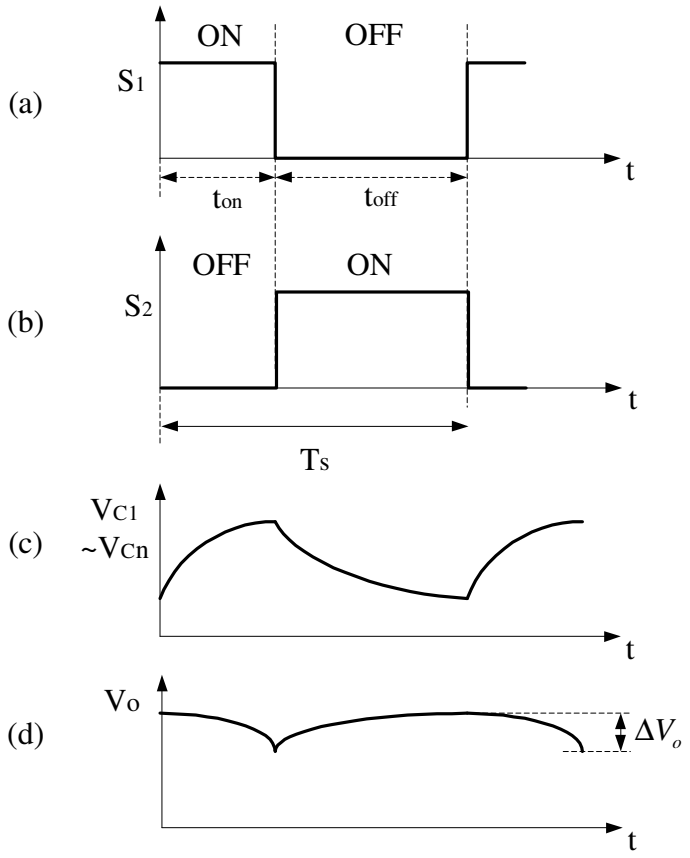
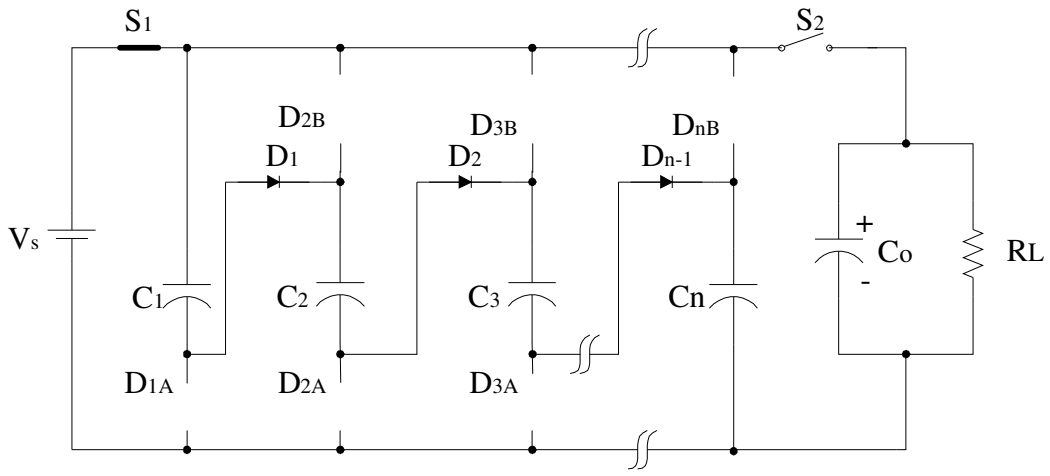
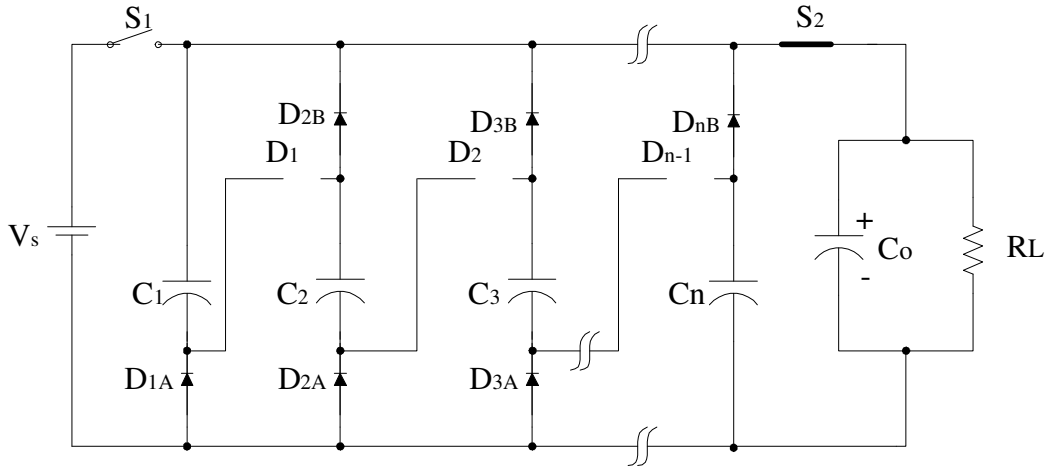


Fig. 2.8. Conventional n-stage step-down charge pump timing diagram and waveforms.
(a) Driving signal for S_1
(b) Driving signal for S_2
(c) Voltages across capacitors C_1~C_n
(d) Output voltage ripple



(a) Charging interval



(b) Discharging interval

Fig. 2.9. Switching states of the conventional n-stage step-down charge pump.

Fig. 2.10 shows a circuit that was proposed in [40]. As can be seen, the circuit consists of two identical step-down charge pump cells. While one cell is being charged, the other one will be discharged, and vice versa. Therefore, this is actually using the interleaving technique. The circuit has a total of four states. Fig. 2.11

illustrates the circuit topologies during state 1 and state 2. State 3 and state 4 are similar to state 1 and 2, only that the function of cell 1 and cell 2 are interchanged. Several other papers also employed the interleaving technique, as in [41], [42].

The analysis method that is suitable for dc-dc switching converters is state-space averaging (SSA), which was first proposed by Middlebrook and Ćuk in 1976 [43]. The SSA includes the following steps:

1) Determine the different operating states of the dc-dc converter
2) Establish the state-space equations for each operating state

$$\dot{X}(t) = A_k X(t) + B_k U ,$$
$$Y(t) = C_k X(t) \tag{2-2}$$

Note that it is convenient to choose inductor currents and capacitor voltages as the state variables.

3) Obtain the weighted-average of the above state-space equations

$$\dot{X}(t) = AX(t) + BU = \sum_k d_k A_k X(t) + \sum_k d_k B_k U ,$$
$$Y(t) = CX(t) = \sum_k d_k C_k X(t) \tag{2-3}$$

Where the weight d_k is the ratio of each switching interval t_k to the switching period T_s.

4) Then the steady-state dc model of the dc-dc converter is

$$X(t) = -A^{-1}BU$$
$$Y(t) = CX(t) = -CA^{-1}BU \tag{2-4}$$

After applying the state-space averaging, the steady state output voltage of the charge pump in Fig. 2.10 is expressed as [40]

$$V_o = \frac{V_s - 3V_d}{2 + Y_L(\frac{1}{g_2} + \frac{1}{4g_1 D})} = \frac{V_s - 3V_d}{2 + \frac{1}{R_L}[(2r_2 + r) + \frac{2r + r_1}{4D}]} \tag{2-5}$$

Where r is the equivalent series resistance (ESR) of the capacitors, r_1 is the on-resistance of the p-type MOSFETs, r_2 is the on-resistance of the n-type MOSFETs, and D is the steady-state value of the duty ratio of S_1 and S_3.

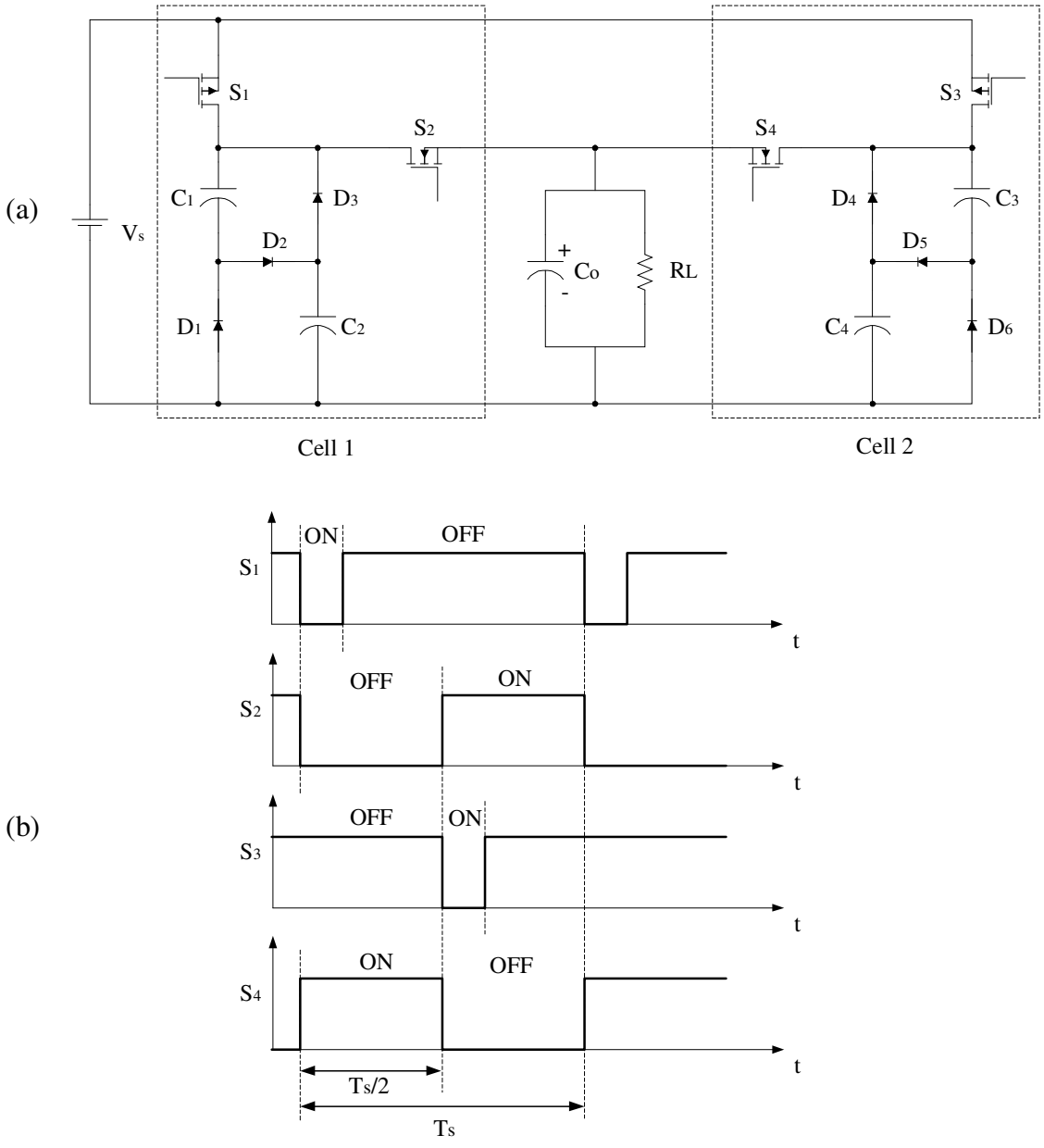


Fig. 2.10. Step-down charge pump in [40].
(a) circuit, and (b) its timing diagram

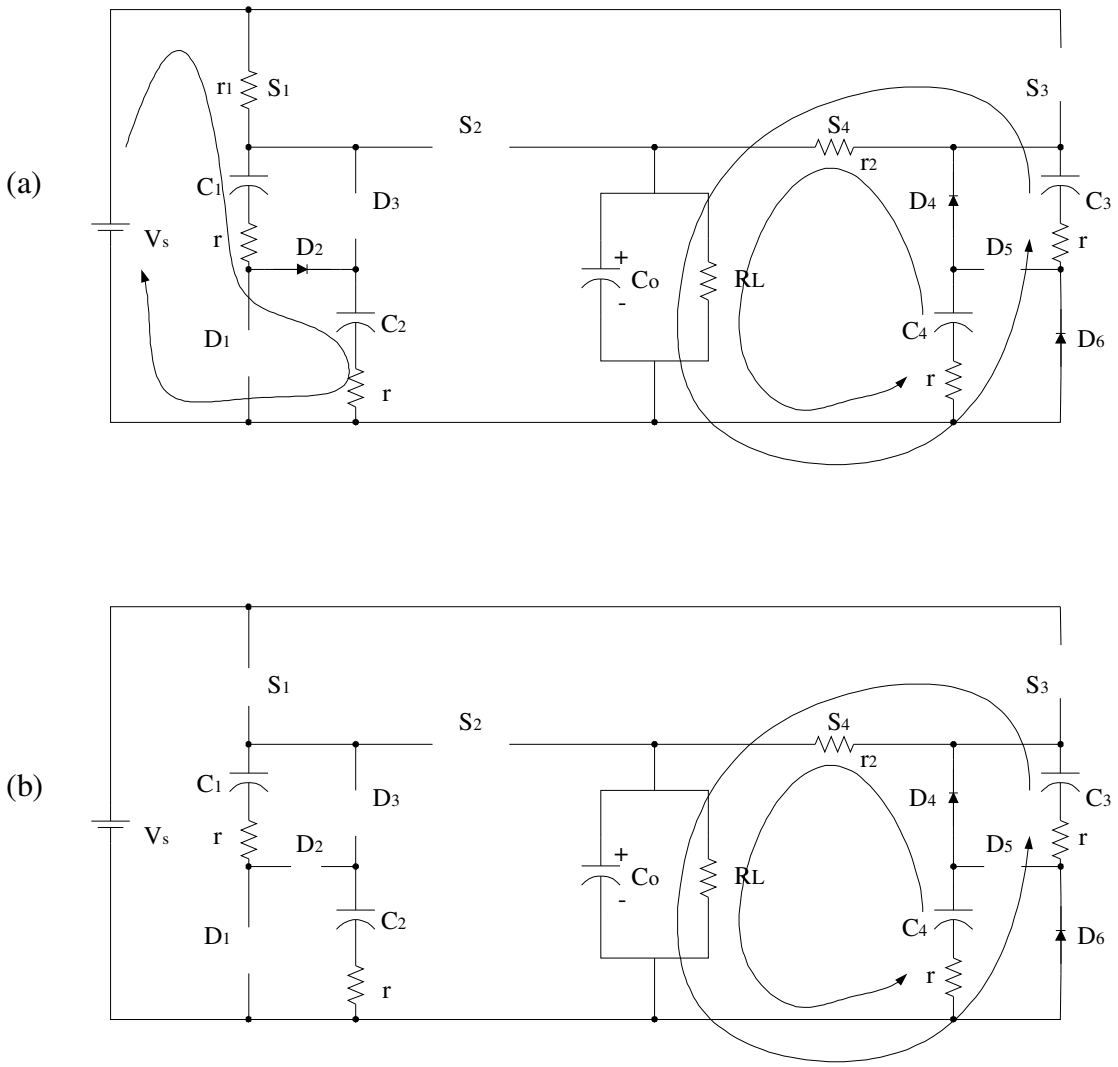


Fig. 2.11. Switching states of the charge pump in [40].
(a) State 1, (b) State 2

2.3.2 Proposed Step-Down Charge Pump with Interleaved Discharge

This work proposes a new approach to controlling the capacitor discharging process in a step-down charge pump. Unlike in a conventional step-down charge pump where the capacitors are discharged simultaneously, in the proposed step-down charge pump the capacitors are discharged one-by-one, which is called interleaved discharge

(ID) here. For an n-stage step-down charge pump (i.e., the step-ratio is n), the interleaved discharging process is realized by introducing a phase shift of $2\pi/n$ to each capacitor during the discharging period. The capacitors are discharged one after another. Therefore, by applying the ID method we could obtain an output ripple with a frequency of nT_S. Since the output voltage ripple is inversely proportional to the ripple frequency, the output ripple can be reduced by n times without requiring extra power switches and capacitors.

The proposed ID method is also a kind of interleaving technique. However, it is different from the conventional interleaving technique. The ID method takes full advantage of the special structure of the step-down charge pumps, and it does not need any extra converter cells, recalling Fig. 2.2. The ID method does need some extra driving signals for the switches, but some simple circuits such as flip-flops can generate these signals.

The schematic of the proposed n-stage charge pump is shown in Fig. 2.12. It can be noticed that the component count of the power stage is the same as that in Fig. 2.7, with some of the diodes replaced by MOSFETs. In order to obtain high efficiency in low-voltage low-power applications, all the diodes should be replaced by power switches, even in conventional charge pumps. For medium power charge pumps, replacing the diodes with MOSFETs can still improve the efficiency. In fact, the power stage (not including the control circuit) in Fig. 2.12 is similar to that of a 48W charge pump presented in [17]. It should be pointed out that the power switches (in Fig. 2.12) that replace the original diodes (in Fig. 2.7) would not present difficulties since it is possible to integrate power switches on chip in low-power applications. Also, floating diodes are difficult to realize in complementary metal-oxide semiconductor (CMOS) technology. Fig. 2.13 shows the switching states of the proposed n-stage step-down charge pump. Only discharging interval 1 is shown in Fig. 2.13 (b), since other discharging intervals are all similar, except the $2\pi/n$ phase shifts.

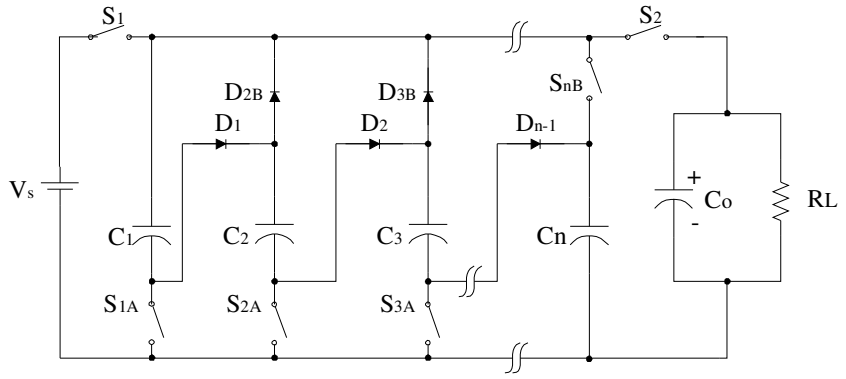
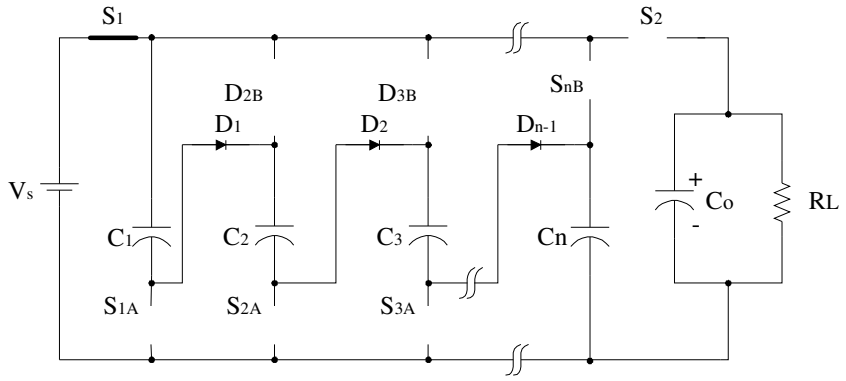
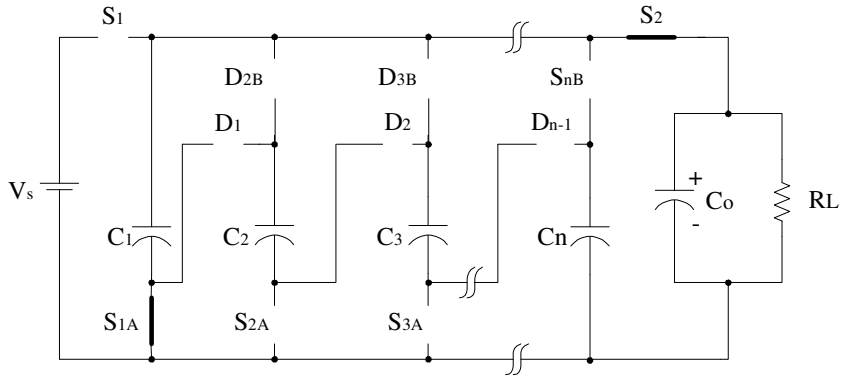


Fig. 2.12. Proposed step-down charge pump with interleaved discharge.



(a) Charging interval



(b) Discharging interval 1

Fig. 2.13. Switching states of the proposed charge pump.

Fig. 2.14 shows the timing diagram and waveforms for the proposed charge pump. It can be seen that when C_1 is being discharged, other capacitors are untouched, i.e., their voltages are kept constant (neglect the leakage current). The similar process is repeated by other capacitors till the end of t_{off}. Compared with Fig. 2.8 (d), the output voltage in Fig. 2.14 (f) has higher frequency and reduced peak-to-peak ripple.

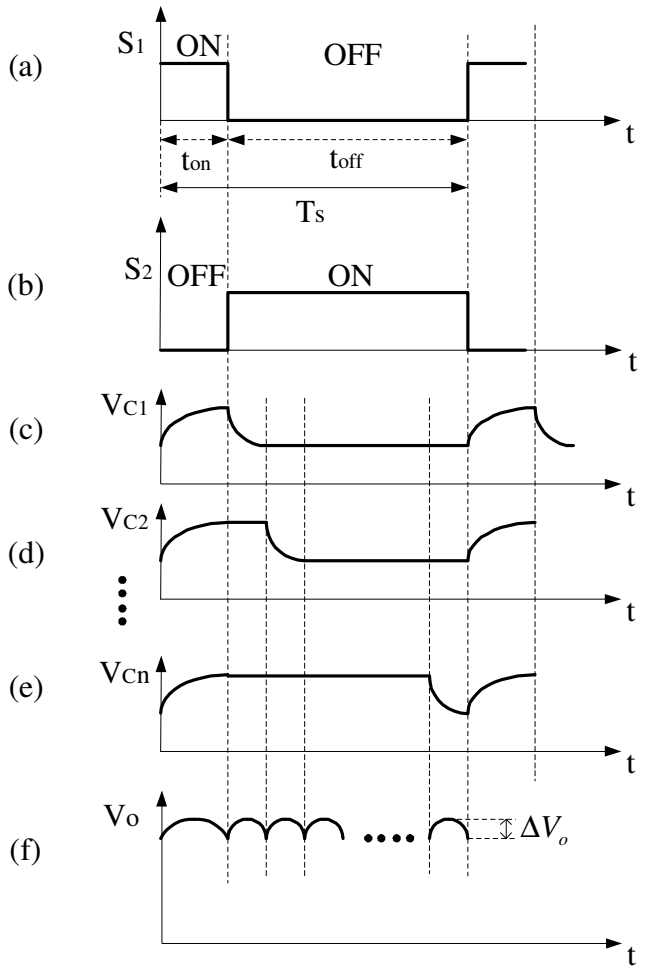


Fig. 2.14. Proposed timing diagram and waveforms.

In order to verify the proposed interleave discharge method, it is applied to the circuit in Fig. 2.10 (a). Fig. 2.15 shows the circuit with the ID method. The timing diagram is shown in Fig. 2.16. Suppose the diodes are replaced with switches that also

have a voltage drop of V_d, so that we can make a fair comparison with the steady-state output voltage in (2-5).

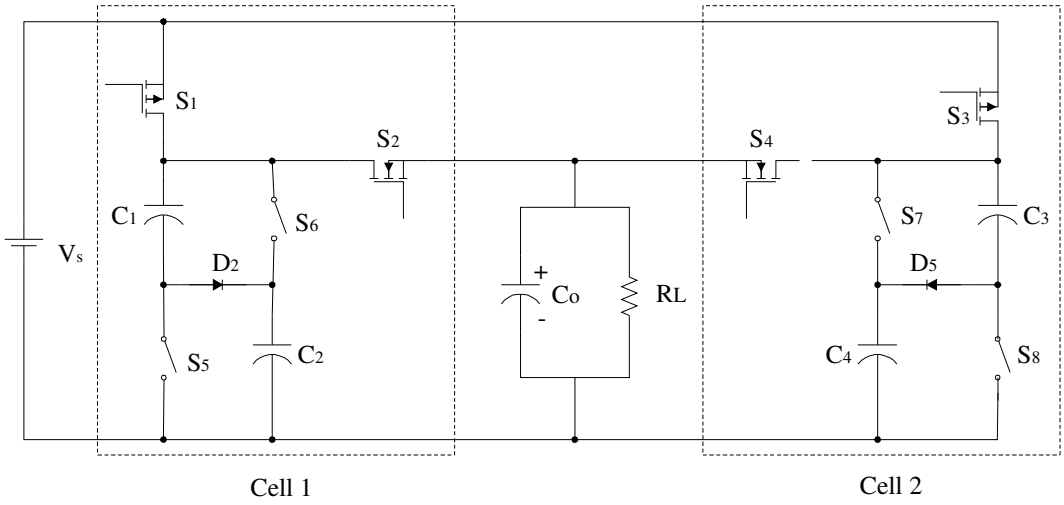


Fig. 2.15. Proposed ID method applied to Fig. 2.10 (a).

Suppose the charging time t_{on} is less than $T_s/4$, such that there will be a total of six switching states. Let the state variables represent the voltages of the five capacitors. Thus,

$$X = [V_{C1} \quad V_{C2} \quad V_{C3} \quad V_{C4} \quad V_{Co}] = [x_1 \quad x_2 \quad x_3 \quad x_4 \quad x_5]^T,$$
$$U = [V_s \quad V_d]^T \tag{2-6}$$

The state equations for each switching state is:

$$\dot{X}(t) = A_k X(t) + B_k U, \quad \text{k=1,2,…6} \tag{2-7}$$

The switching configurations during switching states 1~6 are shown in Fig. 2.17 (a)~(f), respectively. Fig. 2.15 is analyzed as follows.

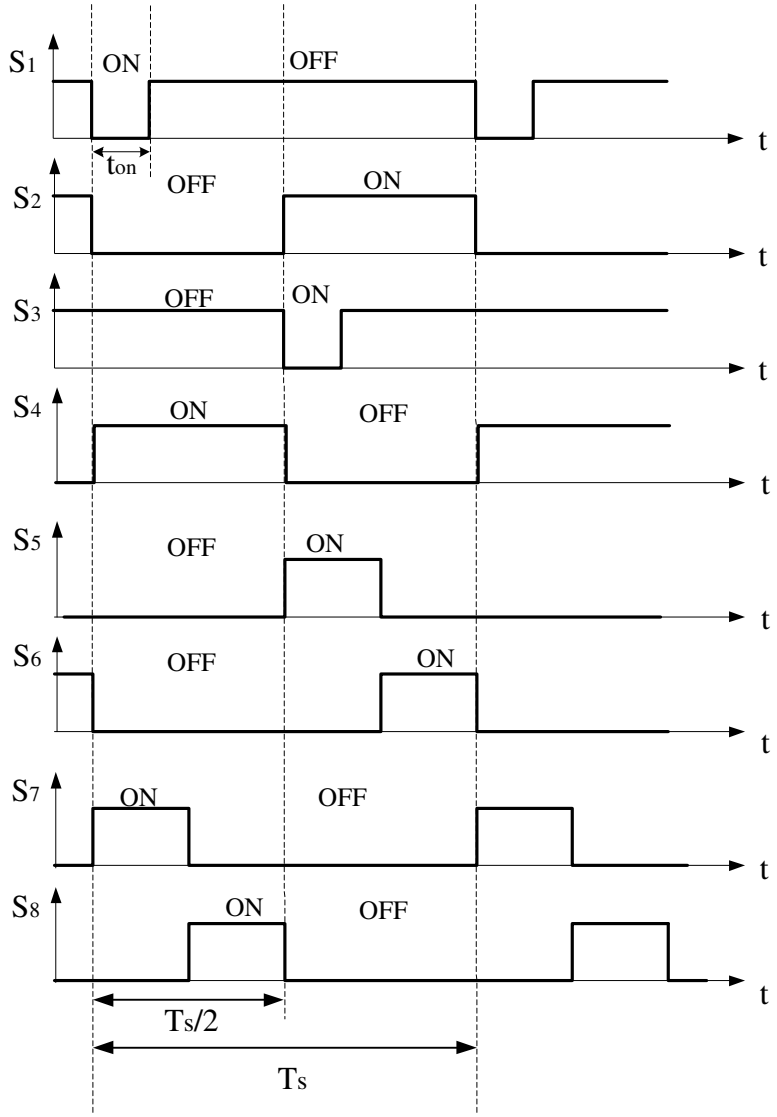


Fig. 2.16. Timing diagram of Fig. 2.15.

1) State 1: Capacitors C_1 and C_2 are charged in series through S_1 and D_2. At the same time, C_4 is discharged through S_4 and S_7. By applying KVL, we obtain the following

$$C\frac{dx_1}{dt} = \frac{V_s - V_d - x_1 - x_2}{2r + r_1}$$

$$C\frac{dx_2}{dt} = \frac{V_s - V_d - x_1 - x_2}{2r + r_1}$$

$$-C\frac{dx_3}{dt} = \frac{x_s - V_d - x_5}{r + r_2}$$

$$C_o\frac{dx_5}{dt} + \frac{x_5}{R_L} = \frac{x_3 - V_d - x_5}{r + r_2} \tag{2-8}$$

By rearranging the above equations, we obtain the following matrices for state 1:

$$A_1 = \begin{bmatrix} -\frac{g_1}{C} & -\frac{g_1}{C} & 0 & 0 & 0 \\ -\frac{g_1}{C} & -\frac{g_1}{C} & 0 & 0 & 0 \\ 0 & 0 & -\frac{g_2}{C} & 0 & \frac{g_2}{C} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{g_2}{C_o} & 0 & -\frac{g_2}{C_o} - \frac{Y}{C_o} \end{bmatrix}, \qquad B_1 = \begin{bmatrix} \frac{g_1}{C} & -\frac{g_1}{C} \\ \frac{g_1}{C} & -\frac{g_1}{C} \\ 0 & \frac{g_2}{C} \\ 0 & 0 \\ 0 & -\frac{g_2}{C_o} \end{bmatrix} \tag{2-9}$$

2) State 2: C_4 is still discharged through S_4 and S_7. By applying KVL, we obtain the following

$$-C\frac{dx_3}{dt} = \frac{x_s - V_d - x_5}{r + r_2}$$

$$C_o\frac{dx_5}{dt} + \frac{x_5}{R_L} = \frac{x_3 - V_d - x_5}{r + r_2} \tag{2-10}$$

The matrices for the state equation are thus

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{g_2}{C} & 0 & \frac{g_2}{C} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{g_2}{C_o} & 0 & -\frac{g_2}{C_o} - \frac{Y}{C_o} \end{bmatrix}, \qquad B_2 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & \frac{g_2}{C} \\ 0 & 0 \\ 0 & -\frac{g_2}{C_o} \end{bmatrix} \tag{2-11}$$

3) State 3: C_3 is discharged through S_4 and S_8. By applying KVL, we obtain the following

$$-C\frac{dx_4}{dt} = \frac{x_4 - V_d - x_5}{r + r_2}$$

$$C_o\frac{dx_5}{dt} + \frac{x_5}{R_L} = \frac{x_4 - V_d - x_5}{r + r_2} \tag{2-12}$$

By rearranging the above equations, we obtain the following matrices for state 3:

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{g_2}{C} & \frac{g_2}{C} \\ 0 & 0 & 0 & \frac{g_2}{C_o} & -\frac{g_2}{C_o} - \frac{Y}{C_o} \end{bmatrix}, \qquad B_3 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{g_2}{C} \\ 0 & -\frac{g_2}{C_o} \end{bmatrix} \tag{2-13}$$

4) State 4: Capacitors C_3 and C_4 are charged in series through S_3 and D_5. At the same time, C_1 is discharged through S_2 and S_5. By applying KVL, we obtain the following

$$C\frac{dx_3}{dt} = \frac{V_s - V_d - x_3 - x_4}{2r + r_1}$$

$$C\frac{dx_4}{dt} = \frac{V_s - V_d - x_3 - x_4}{2r + r_1}$$

$$-C\frac{dx_1}{dt}=\frac{x_1-V_d-x_5}{r+r_2}$$

$$C_o\frac{dx_5}{dt}+\frac{x_5}{R_L}=\frac{x_1-V_d-x_5}{r+r_2} \tag{2-14}$$

Therefore, we have the following matrices for the state equation in state 4:

$$A_4=\begin{bmatrix} -\frac{g_2}{C} & 0 & 0 & 0 & \frac{g_2}{C} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{g_1}{C} & -\frac{g_1}{C} & 0 \\ 0 & 0 & -\frac{g_1}{C} & -\frac{g_1}{C} & 0 \\ \frac{g_2}{C_o} & 0 & 0 & 0 & -\frac{g_2}{C_o}-\frac{Y}{C_o} \end{bmatrix}, \qquad B_4=\begin{bmatrix} 0 & \frac{g_2}{C} \\ 0 & 0 \\ \frac{g_1}{C} & -\frac{g_1}{C} \\ \frac{g_1}{C} & -\frac{g_1}{C} \\ 0 & -\frac{g_2}{C_o} \end{bmatrix} \tag{2-15}$$

5) State 5: C_1 is still discharged through S_2 and S_5. By applying KVL, we obtain the following

$$-C\frac{dx_1}{dt}=\frac{x_1-V_d-x_5}{r+r_2}$$

$$C_o\frac{dx_5}{dt}+\frac{x_5}{R_L}=\frac{x_1-V_d-x_5}{r+r_2} \tag{2-16}$$

The matrices in the state equation for state 5 are

$$A_5=\begin{bmatrix} -\frac{g_2}{C} & 0 & 0 & 0 & \frac{g_2}{C} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{g_2}{C_o} & 0 & 0 & 0 & -\frac{g_2}{C_o}-\frac{Y}{C_o} \end{bmatrix}, \qquad B_5=\begin{bmatrix} 0 & \frac{g_2}{C} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{g_2}{C_o} \end{bmatrix} \tag{2-17}$$

6) State 6: C_2 is discharged through S_2 and S_6. By applying KVL, we obtain the following

$$-C\frac{dx_2}{dt} = \frac{x_2 - V_d - x_5}{r + r_2}$$

$$C_o\frac{dx_5}{dt} + \frac{x_5}{R_L} = \frac{x_2 - V_d - x_5}{r + r_2} \tag{2-18}$$

The matrices in the state equation for state 6 are

$$A_6 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{g_2}{C} & 0 & 0 & \frac{g_2}{C} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{g_2}{C_o} & 0 & 0 & -\frac{g_2}{C_o} - \frac{Y}{C_o} \end{bmatrix}, \qquad B_6 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{g_2}{C} \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{g_2}{C_o} \end{bmatrix} \tag{2-19}$$

The duty ratio is defined as $D = \frac{t_{on}}{T_S}$. By applying the weighted-average of the above state-space matrices, we obtain the matrices for the averaged state-space equations:

$$A_{av} = \begin{bmatrix} -\frac{Dg_1}{C} - \frac{g_2}{4C} & -\frac{Dg_1}{C} & 0 & 0 & \frac{g_2}{4C} \\ -\frac{Dg_1}{C} & -\frac{Dg_1}{C} - \frac{g_2}{4C} & 0 & 0 & \frac{g_2}{4C} \\ 0 & 0 & -\frac{Dg_1}{C} - \frac{g_2}{4C} & -\frac{Dg_1}{C} & \frac{g_2}{4C} \\ 0 & 0 & -\frac{Dg_1}{C} & -\frac{Dg_1}{C} - \frac{g_2}{4C} & \frac{g_2}{4C} \\ \frac{g_2}{4C_o} & \frac{g_2}{4C_o} & \frac{g_2}{4C_o} & \frac{g_2}{4C_o} & -\frac{g_2}{C_o} - \frac{Y}{C_o} \end{bmatrix},$$

$$B_{av} = \begin{bmatrix} \frac{Dg_1}{C} & -\frac{Dg_1}{C} + \frac{g_2}{4C} \\ \frac{Dg_1}{C} & -\frac{Dg_1}{C} + \frac{g_2}{4C} \\ \frac{Dg_1}{C} & -\frac{Dg_1}{C} + \frac{g_2}{4C} \\ \frac{Dg_1}{C} & -\frac{Dg_1}{C} + \frac{g_2}{4C} \\ 0 & -\frac{g_2}{C_o} \end{bmatrix} \tag{2-20}$$

Applying (2-4), we then obtain the steady-state output voltage as

$$V_o = \frac{V_s - 3V_d}{2 + Y_L(\frac{2}{g_2} + \frac{1}{4g_1 D})} = \frac{V_s - 3V_d}{2 + \frac{1}{R_L}[2(r_2 + r) + \frac{2r + r_1}{4D}]} \tag{2-21}$$

It can be observed that the only difference between (2-5) and (2-21) is that the second term in the denominator of (2-21) contains one more r (i.e., capacitor ESR). Since $r/R_L << 1$, the steady-state output voltage of the ID-based charge pump is very close to that of [38], shown in (2-5).

Since the output power of the charge pump is

$$P_o = \frac{V_o^2}{R_L} \tag{2-22}$$

The efficiency of the charge pump is

$$\eta = \frac{P_o}{P_{in}} \tag{2-23}$$

Therefore, the efficiency of the ID-based charge pump should be very close to that of the conventional charge pump, which means that the ID method does not sacrifice the converter efficiency.

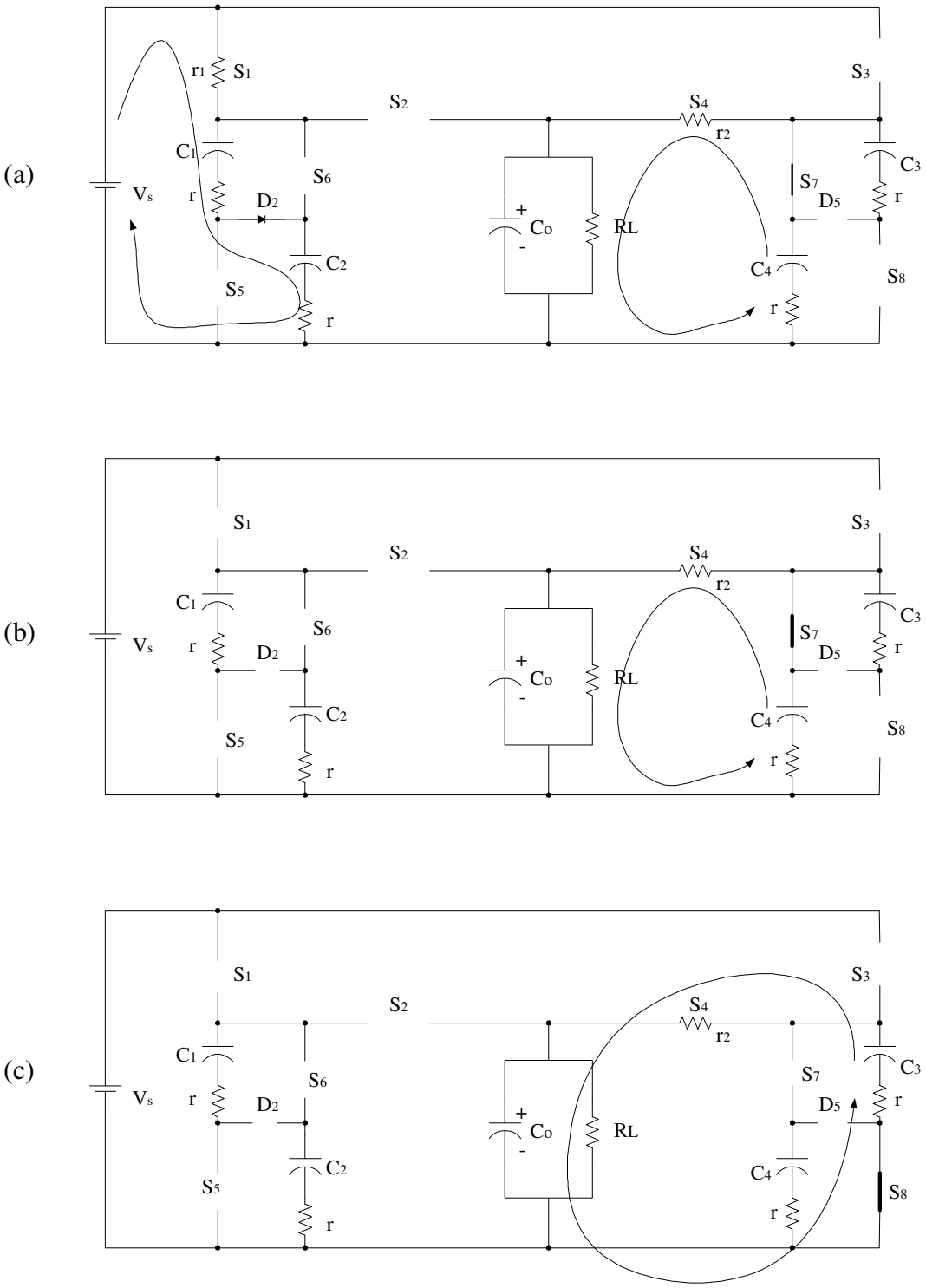
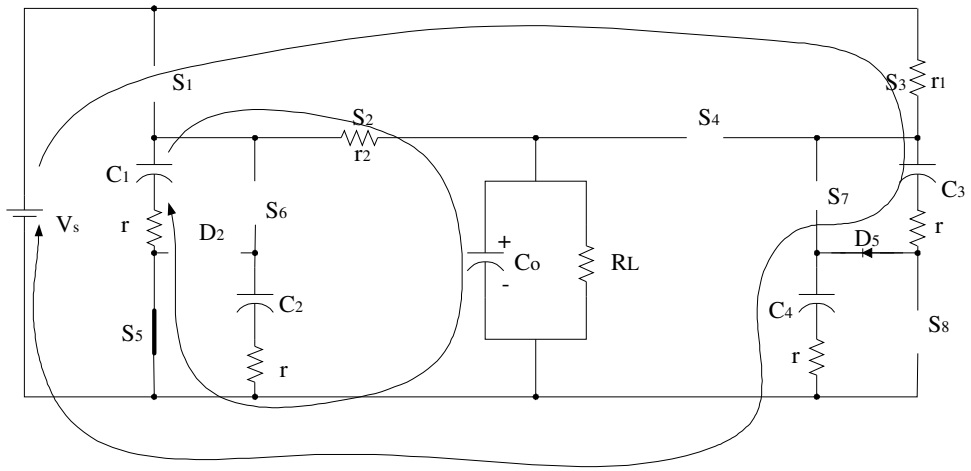
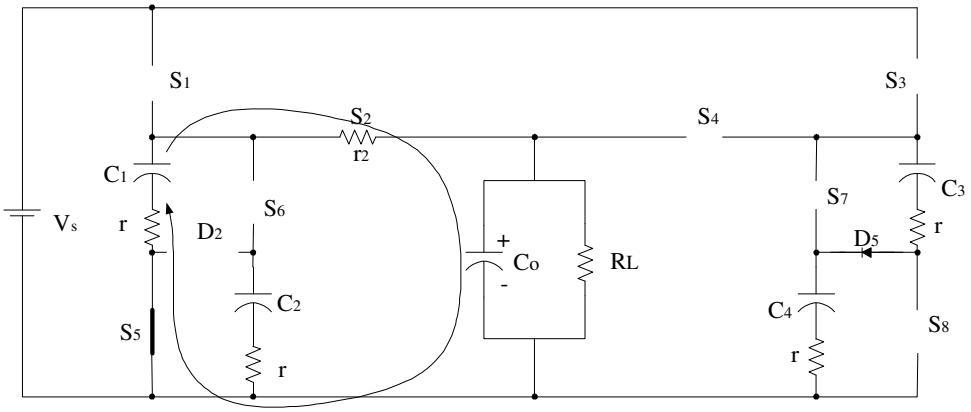


Fig. 2.17. Switching states of the charge pump in Fig. 2.15.
(a)~(c): state 1~3

(d)



(e)



(f)

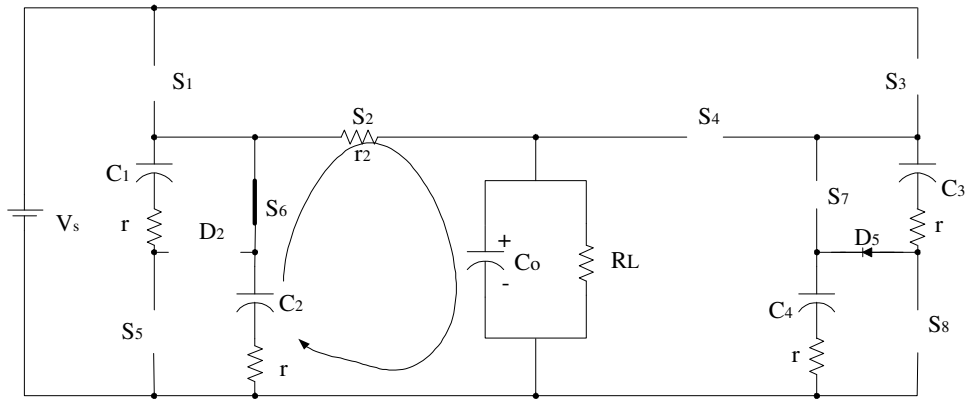


Fig. 2.17. Switching states of the charge pump in Fig. 2.15 (continued).
(d)~(f): state 4~6

In order to show the effectiveness of the interleaved discharge, the charge pump proposed in [17] is simulated here. Fig. 2.18 shows the circuit of the original charge pump. The PSpice simulation waveforms are given in Fig. 2.19.

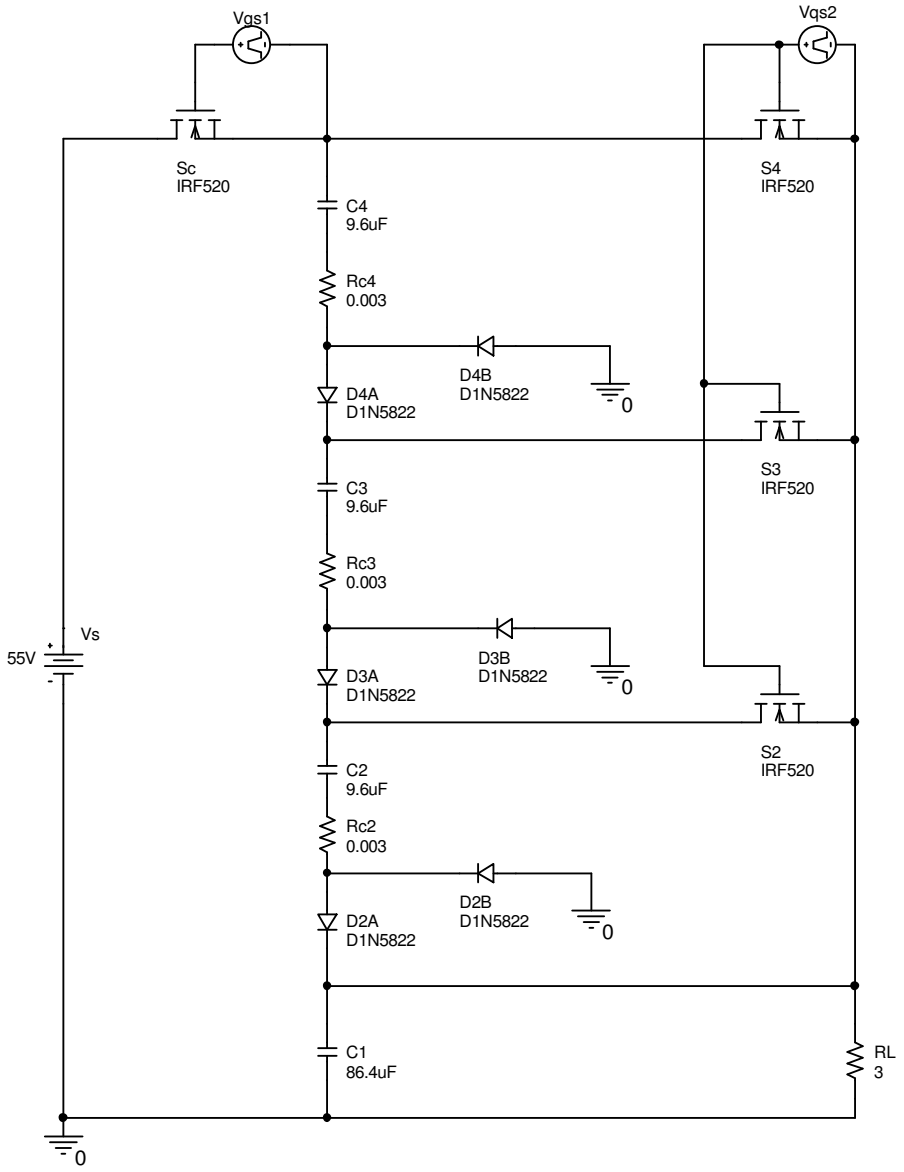


Fig. 2.18. Charge pump proposed in [17].

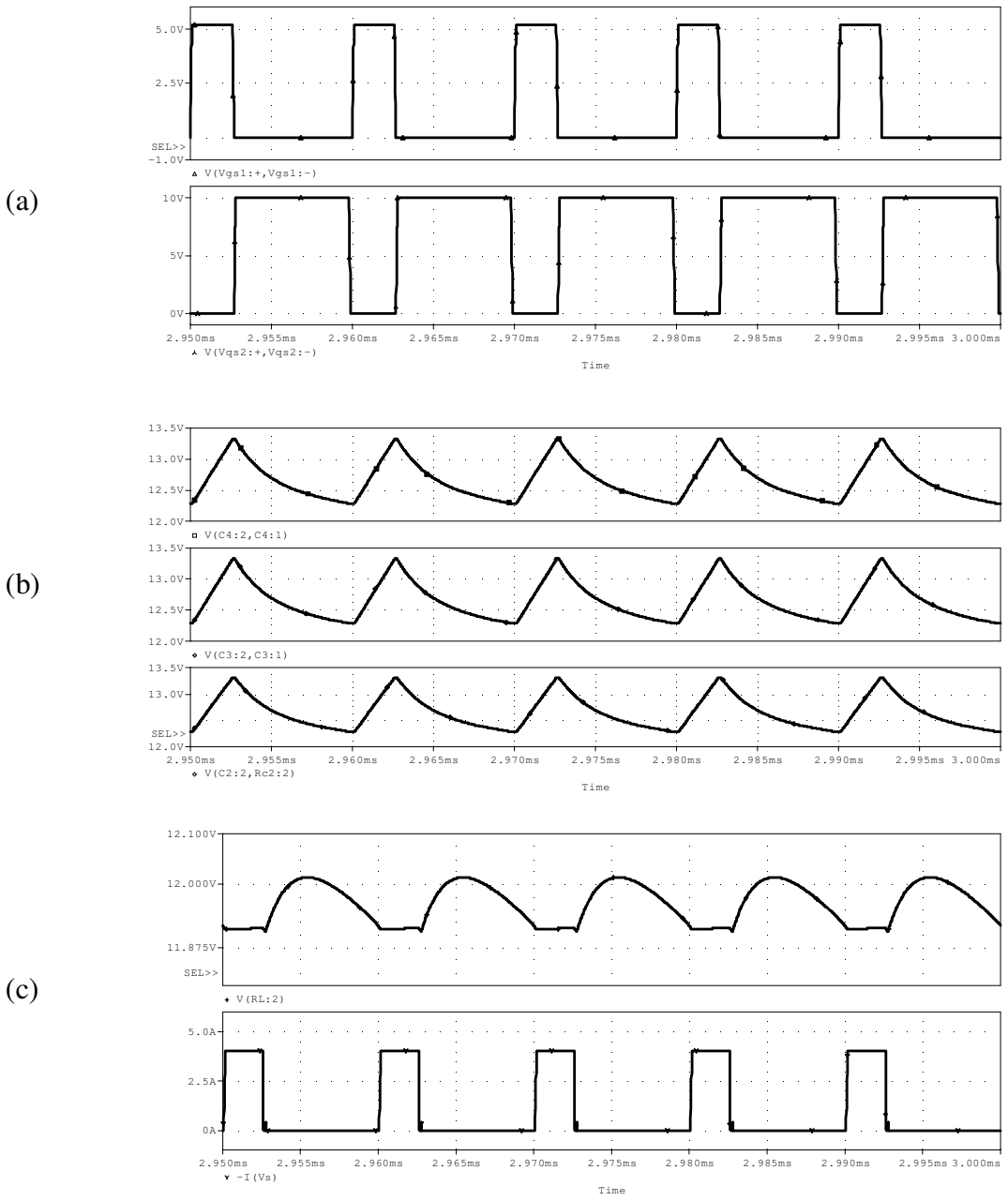


Fig. 2.19. Simulation results of the original charge pump in [17].
(a) Gate driving signal for S_c (upper) and S_2~S_4 (bottom), (b) Capacitor voltages, and (c) Output voltage (upper) and input current (bottom).

Fig. 2.20 shows the circuit applying the ID method. The corresponding waveforms are shown in Fig. 2.21. Note the phase shift in Fig. 2.21 (a) and (b).

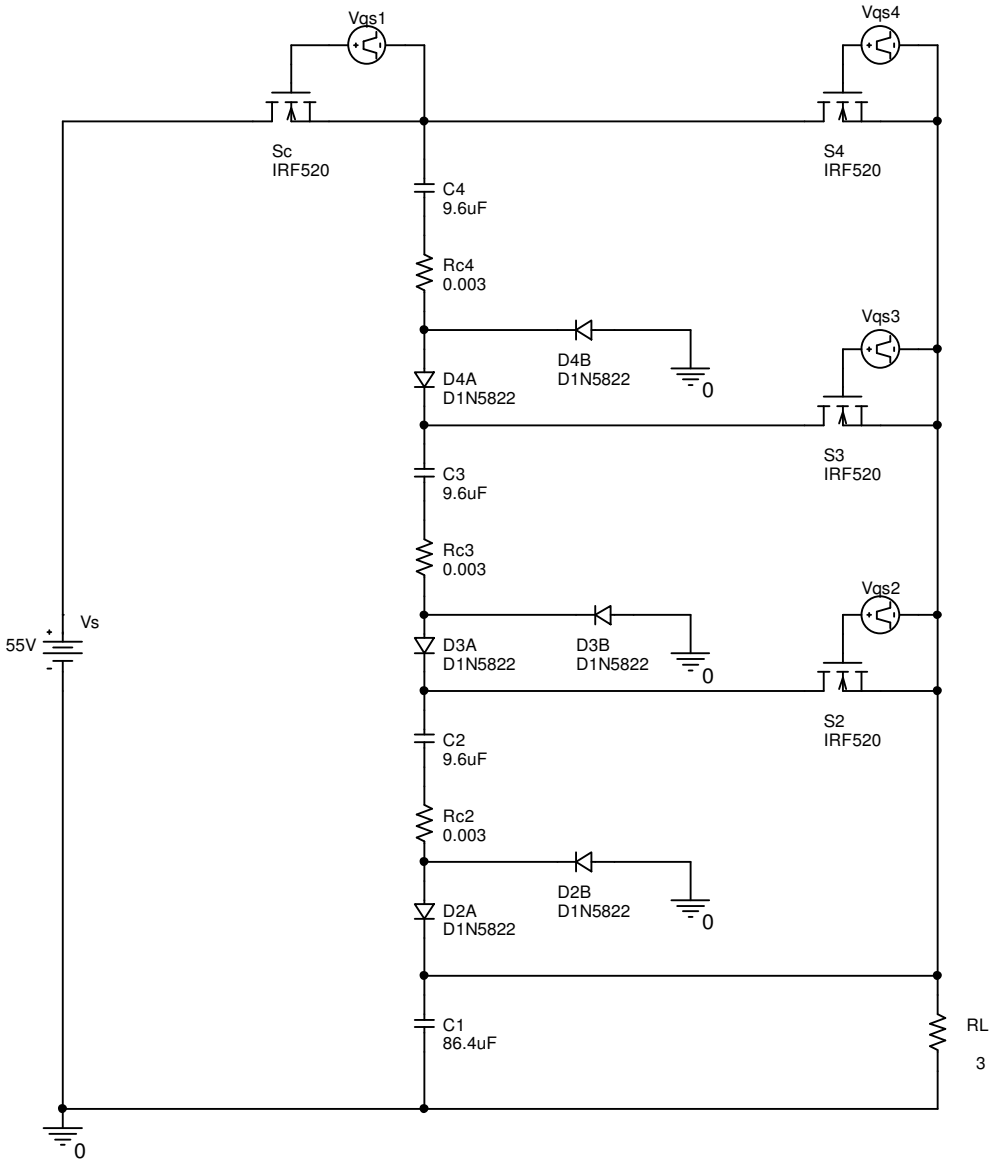


Fig. 2.20. Charge pump using the proposed ID method.

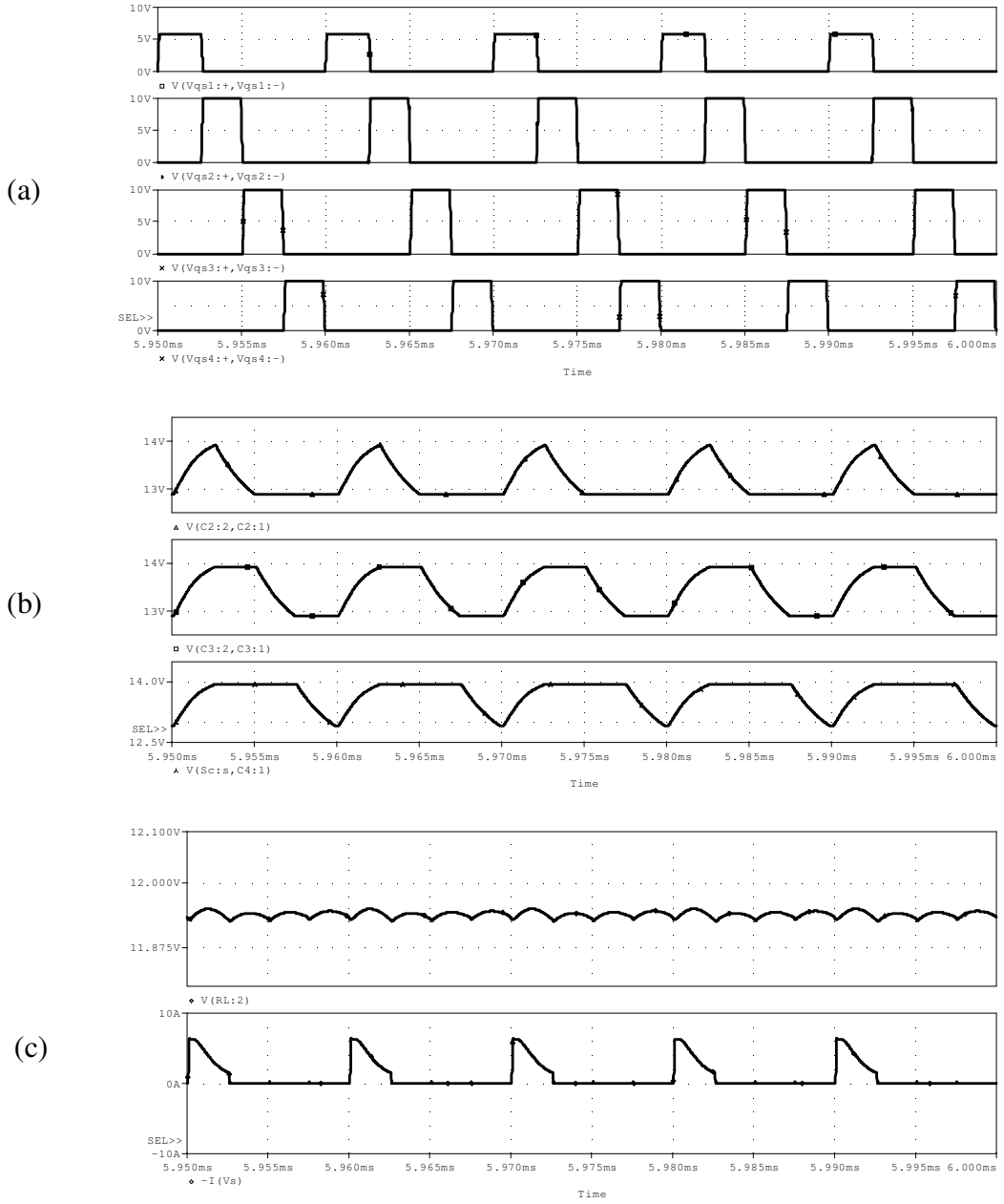


Fig. 2.21. Simulation results of the charge pump using ID method.
(a) Gate driving signal for S_c and S_2~S_4 (top to bottom), (b) Capacitor voltages, and (c) Output voltage (upper) and input current (bottom).

The simulation results of both cases are compared in Table 2.3. It is shown that the proposed ID method can reduce the output ripple greatly, while not sacrificing other circuit parameters. Note that the switching frequencies for both cases are 100kHz.

Table 2.3 Simulation results of the conventional charge pump and the proposed charge pump.

	Average Output voltage (V)	Average Input current (A)	Efficiency (%)	Ripple (mV)
Original	11.959	1.013	85.6	106
Proposed	11.940	1.008	85.7	24

The proposed ID method provides some flexibility in designing charge pumps. If the ripple requirement has already been met, we can use this technique for other benefits such as to:

1) Reduce the capacitance value of the output filter, for lower cost and higher density, and
2) Reduce the switching frequency for higher efficiency (reduced power switch losses).

All the simulation netlists are given in Appendix A.

2.4 Summary

In this chapter, a novel power conditioning circuit for micro power generators was designed. The rectifier stage and the dc-dc regulator stage were designed separately. Three schemes of the rectifier were presented. The proposed rectifier stage

is based on the synchronous rectification technique. The dc-dc regulator is a charge pump-based step-down converter. Interleaved discharge (ID) is proposed to reduce the output voltage ripple greatly, without sacrificing the converter efficiency. The proposed step-down charge pump is analyzed with state-space averaging. Simulation verifies the superiority of the proposed ID method. The proposed ID method provides flexibility in designing charge pumps.

3 DESIGN SIMULATIONS

In this chapter, possible rectifier topologies in the PCC are simulated with PSpice. In order to facilitate the PZT simulation in PSpice, a simplified PZT model is developed. The output voltage spectrum of the PZT is analyzed with Fast Fourier Transform (FFT) so that the PSpice PZT model can generate the same waveforms as the real PZT membranes. After that, three possible rectifier topologies are simulated with PSpice. A 5V/1.2V, 200mW, 1% output ripple charge pump is also simulated.

3.1 PZT Modeling

3.1.1 Commonly Used PZT Model

In Chapter 1, we have already mentioned the commonly used Van Dyke's model for representing the equivalent circuit of a piezoelectric membrane. For convenience, it is redrawn in Fig. 3.1. The model contains a motional branch (L_1, R_1, C_1) and a static branch (C_0).

S. Sherrit, et al [44] proposed an alternate model, which includes complex circuit components, as shown in Fig. 3.2. This complex circuit model takes into account the dielectric and piezoelectric loss as well as the mechanical loss found in the Van Dyke's model. However, there is no resistance element in the motional branch, and the losses associated with the vibrator are represented as imaginary components of C_1, L_1, and C_0. This model is difficult to handle with in PSpice simulations, since the capacitance values of C_1 and C_0, and the inductance value of L_1 are complex numbers.

For both the above-mentioned PZT models, in order to obtain the electrical circuit components, we need to know many material parameters of the PZT membrane, i.e., the elastic, piezoelectric, and electromechanical constants, etc. Worst

of all, some of the parameters may be difficult for PCC designers to obtain. Therefore, it is desirable to develop a model that is suitable for PCC design, without resorting to those complicated parameters.

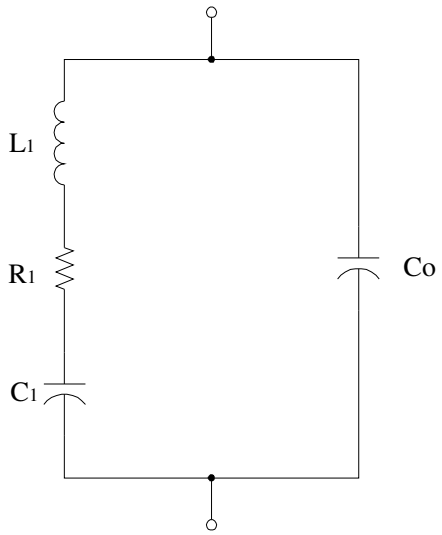


Fig. 3.1. Equivalent model of the piezoelectric generator (Van Dyke's model).

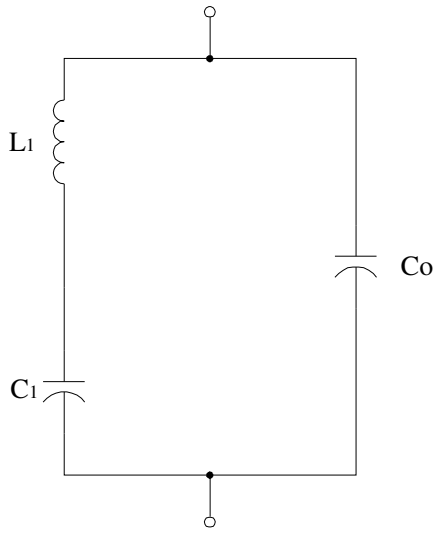


Fig. 3.2. The complex circuit model for PZT [44].

3.1.2 Simplified PZT Model

By observing the Van Dyke's model in Fig. 3.1 we can see that the circuit has two resonance frequencies [38]: a series resonance frequency f_s and a parallel resonance frequency f_p.

$$f_s = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{3-1}$$

$$f_p = \frac{1}{2\pi\sqrt{L_1 \frac{C_1 C_o}{C_1 + C_o}}} \tag{3-2}$$

At f_s, the PZT impedance is minimized. At f_p, the PZT impedance is maximized. The parallel resonance frequency f_p is also known as anti-resonance frequency. For the purpose of power generation, we need the PZT membrane to work at series resonance, in order to obtain maximum output power. Therefore, from the viewpoint of power extraction, instead of using the Van Dyke's model or the complex circuit model, we could develop a simplified model, which considers the series resonance of the circuit. The simplified model is shown in Fig. 3.3.

The parameters in the simplified model can be obtained with an HP4284A Precision LCR Meter. The effectiveness of the simplified model will be verified in a later section. By using this simplified model, PCC designers need not worry about the complicated parameters of the piezoelectric generator. The measured circuit components for the simplified model are as follows

$$C_s = 31.4nF$$

$$R_s = 470\Omega$$

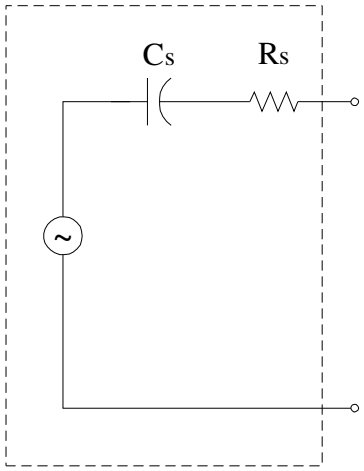


Fig. 3.3. Simplified PZT model.

3.1.3 Maximum Power Extraction

It is desirable to extract maximum power from the PZT membrane. In Fig. 3.4, the power delivered to the load can be expressed as

$$P = |\bar{I}_{rms}|^2 R_L \tag{3-3}$$

In order to obtain maximum power delivery, the internal impedance and the external impedance must be the complex conjugate, i.e.,

$$Z_S = Z_L^* \tag{3-4}$$

Since we have already known that the PZT membrane is capacitive, the matching load should be inductive. From the above-mentioned simplified PZT model, we have

$$X_S = \frac{1}{\omega C_S} = \frac{1}{2\pi f C_S} = \frac{1}{2\times\pi\times 400\times 31.4\times 10^{-9}} = 12671.6\Omega$$

Since $Z_L = \omega L = 2\pi f L$, we obtain

$$L = \frac{Z_L}{2\pi f} = \frac{Z_S}{2\pi f} \approx 5H$$

Obviously, the inductor required is too large for a micro power generator. Therefore, the traditional impedance matching concept is unsuitable for this work.

Instead, we place various resistive loads across the output terminal of the MPG to find the maximum power point. This method is also used in photovoltaic applications [45].

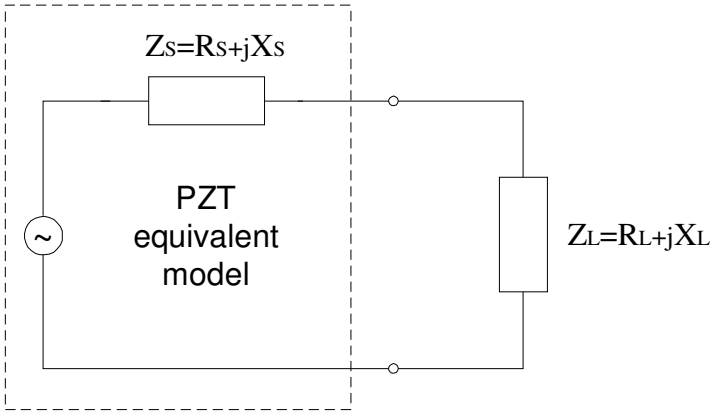
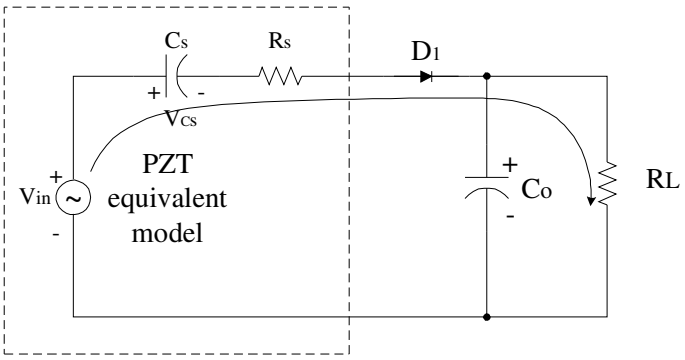


Fig. 3.4. Impedance matching for maximum power transfer.

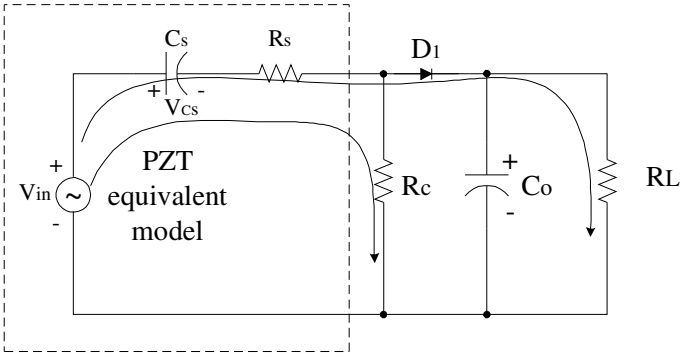
In Chapter 2, it has been shown that there are three schemes for the rectifier stage of the PCC. We mentioned there that a resistor R_c could help us extract more power from the PZT membrane (see Fig. 2.3), which will now be explained. With the above-obtained simplified PZT model, we can redraw scheme I, as shown in Fig. 3.5. In Fig. 3.5 (a), the PZT model is connected directly with the diode rectifier. As can be observed, during the positive half cycle of V_{in}, capacitor C_s will be charged. Depending on the load, it only takes a few cycles to charge C_s to a voltage equal to the magnitude of V_{in}. During the negative half cycle of V_{in}, because the diode is anti-biased, no current is drained from the source, and the voltage across C_s does not change. Then, for the next positive half cycle of V_{in}, V_{Cs} and V_{in} will cancel each other, and no power is extracted from the PZT membrane.

In Fig. 3.5 (b) and (c), a resistor, R_c, is paralleled to the PZT model. During the positive half cycle of V_{in}, i.e., interval 1, capacitor C_s will be charged, and currents

flow through R_c and R_L. During the negative half cycle of V_{in}, i.e., interval 2, the source will charge C_s in the opposite direction, through R_c, as shown in Fig. 3.5 (c). For the next positive half cycle of V_{in}, current will flow through R_L again. Hence, power can be extracted from the PZT membrane. The resistance value of R_c is important. If it is too high, capacitor C_s could not be effectively charged (in the opposite direction) during interval 2; if the resistance is too low, R_c will dissipate a large amount of power during interval 1. Therefore, there exists an optimal resistance value for R_c, which will be explored in section 3.2.

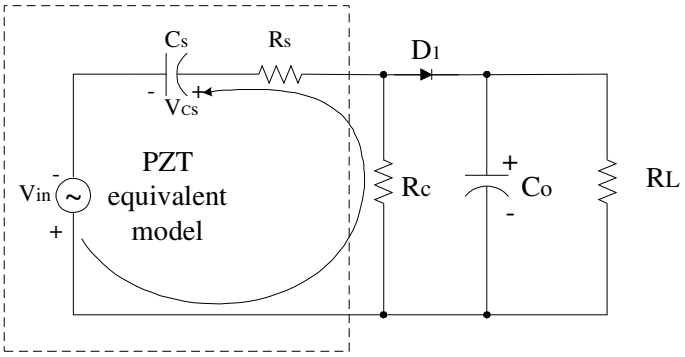


(a) Without R_c



(b) With Rc, interval 1

Fig. 3.5. The function of R_c.



(c) With Rc, interval 2

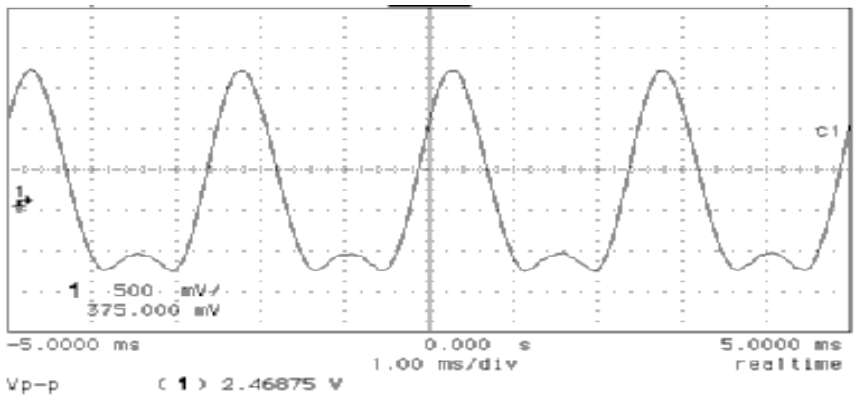
Fig. 3.5. The function of R_c (continued).

3.1.4 Fast Fourier Transform

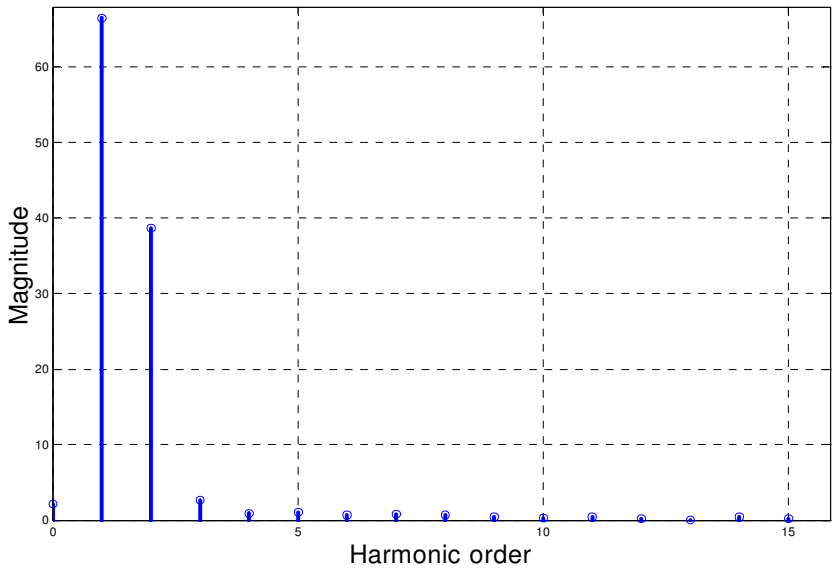
In PSpice simulations, in order to generate the same waveforms as a real P^3 cell, as shown in Fig. 3.6 (a), the harmonic contents of the PZT output waveform were computed with the Matlab command 'fft'. The result is shown in Fig. 3.6 (b). Then, the fundamental and 2^{nd} – 7^{th} harmonics were used to synthesize the PZT waveform in the PSpice simulation. The magnitudes of the fundamental and 2^{nd} – 7^{th} harmonics that were used in the PSpice simulation are tabulated in Table 3.1.

Table 3.1 Magnitudes of the fundamental and 2^{nd} – 7^{th} harmonics.

Order	1	2	3	4	5	6	7
Magnitude (V)	1	0.5822	0.0417	0.0143	0.017	0.0111	0.0122



(a) PZT output voltage waveform under no load



(b) Harmonic contents

Fig. 3.6. FFT of the PZT output waveform.

3.2 Simulation Results for the Rectifier Stage

In Chapter 2, three schemes of the PCC rectifier have been discussed. In this section, they will be verified by PSpice simulation. Various resistive loads were tested

with the PZT model, and an 80kΩ resistive load was found to be able to extract the maximum output power.

3.2.1 Scheme I Simulation Results

The PSpice schematic for scheme I rectifier is shown in Fig. 3.7. In the schematic, voltage sources V_1~V_7 synthesize the fundamental and 2^{nd}-7^{th} harmonics in the PZT membrane output waveform, and their magnitudes are taken from Table 3.1. V_1~V_7, C_S and R_S together represent the simplified PZT model. Fig. 3.8 shows some typical simulation waveforms for scheme I. It is found that $R_c = 40k\Omega$ can lead to the maximum output power of scheme I. By varying the load resistance, we can find the maximum power extraction point. Table 3.2 shows the simulation results. From Table 3.2, we can see that the maximum power of 4.28μW is extracted for an 80kΩ resistive load.

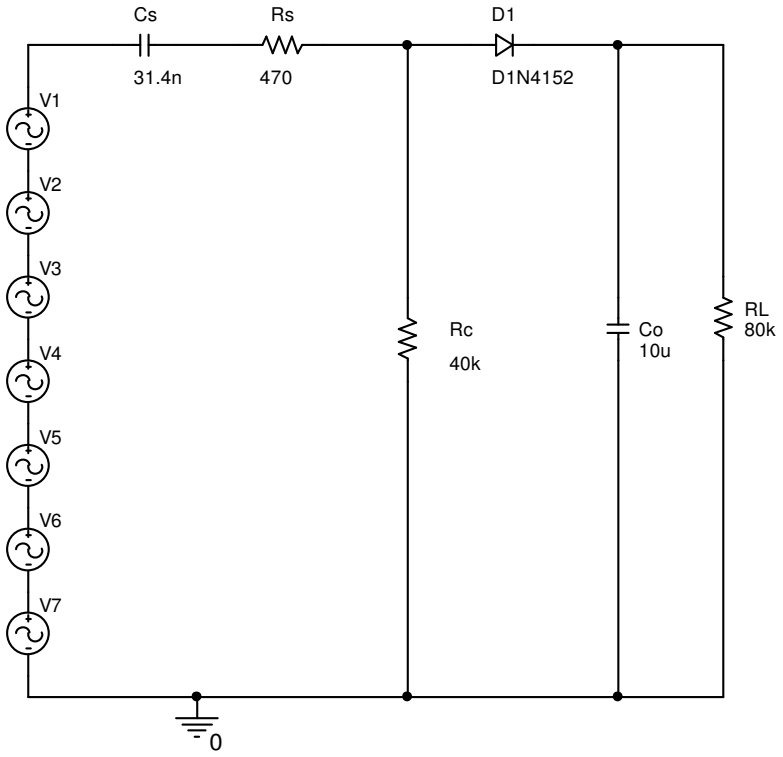
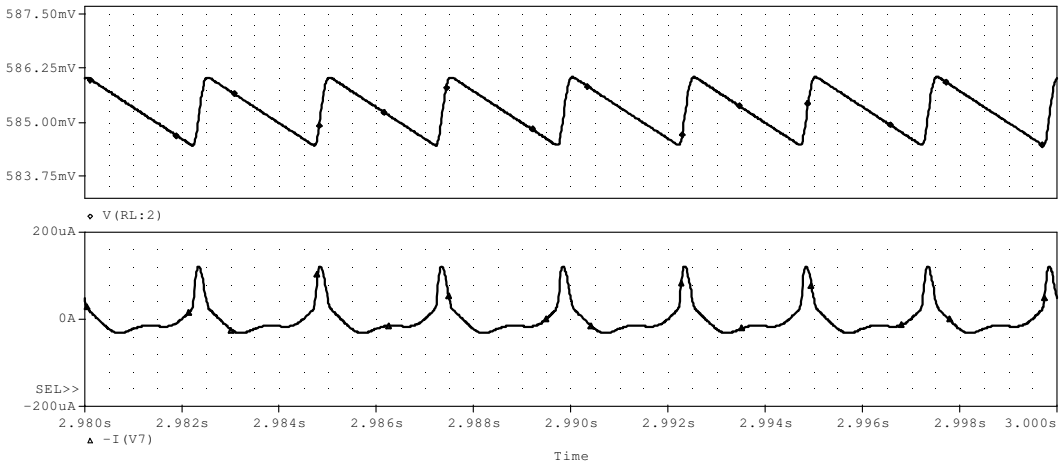
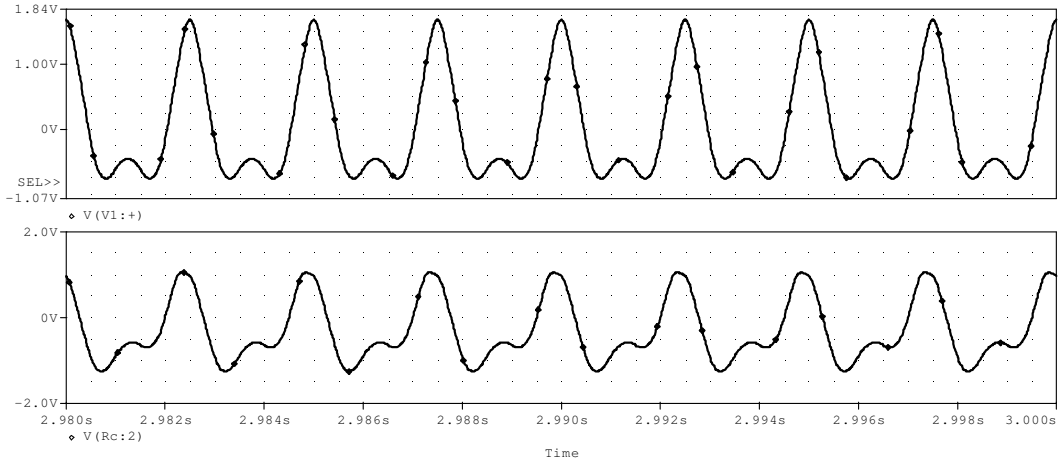


Fig. 3.7. Schematic for PSpice simulation of scheme I rectifier.



(a) Upper: output voltage waveform for an 80kΩ resistive load
Bottom: input current waveform for an 80kΩ resistive load



(b) Upper: PZT model terminal voltage waveform during no load
Bottom: PZT model terminal voltage waveform for an 80kΩ resistive load

Fig. 3.8. Scheme I waveforms from PSpice simulation.

Table 3.2 Scheme I simulation results.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.322	3.46
45	0.423	3.98
52.4	0.464	4.11
63.2	0.517	4.23
67.2	0.535	4.26
70.6	0.549	4.27
80	0.585	4.28
85	0.603	4.27
88.5	0.614	4.26
92	0.626	4.26
97	0.641	4.24
102	0.655	4.21
110	0.677	4.17
129.4	0.722	4.03
139.4	0.742	3.95
154.4	0.769	3.83
184.1	0.814	3.6
196.1	0.83	3.51

In scheme I, both R_c and D_1 are the sources of power losses. Fig. 3.9 shows the waveforms used to analyze the losses of scheme I for an 80kΩ resistive load. Fig. 3.10 shows the output power and loss breakdown of scheme I as a function of load resistance. It can be seen that for loads with high resistance values, the power loss of R_c dominates, and for loads with low resistance values, the power loss of D_1 dominates. When the load is around 80kΩ, the efficiency of scheme I is maximized.

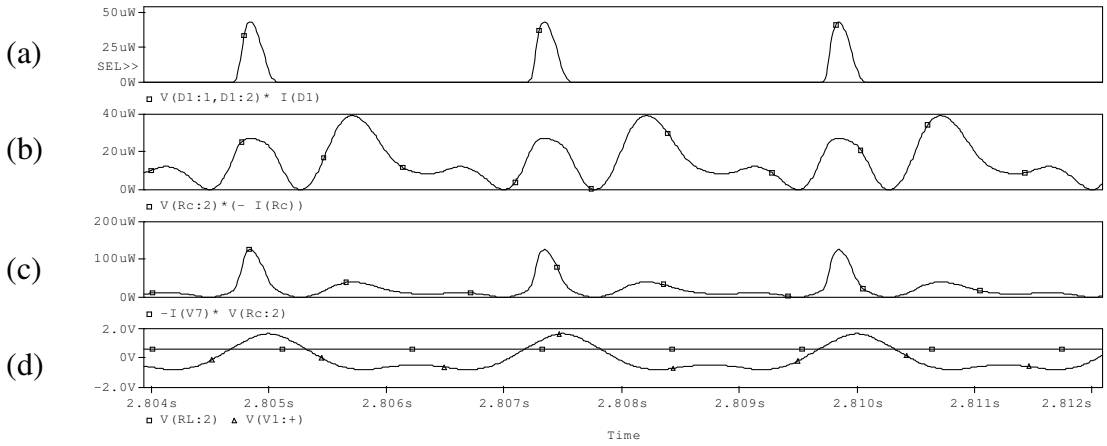


Fig. 3.9. Waveforms for analyzing the losses of scheme I.

(a) Power loss of diode D_1
(b) Power loss of resistor R_c
(c) Total input power to the rectifier stage
(d) Output voltage and PZT output voltage

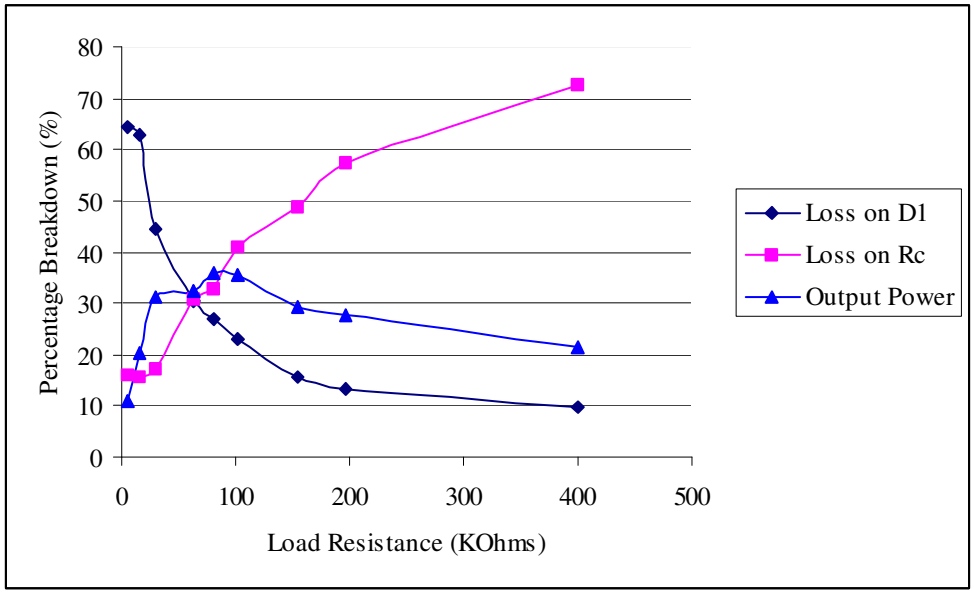


Fig. 3.10. Scheme I output power and loss breakdown.

3.2.2 Scheme II Simulation Results

The PSpice schematic for scheme II rectifier is shown in Fig. 3.11. Fig. 3.12 shows some typical simulation waveforms for scheme II. Scheme II simulation results are listed in Table 3.3. From Table 3.3, we can see that the maximum power of 9.64μW is extracted for an 80kΩ resistive load.

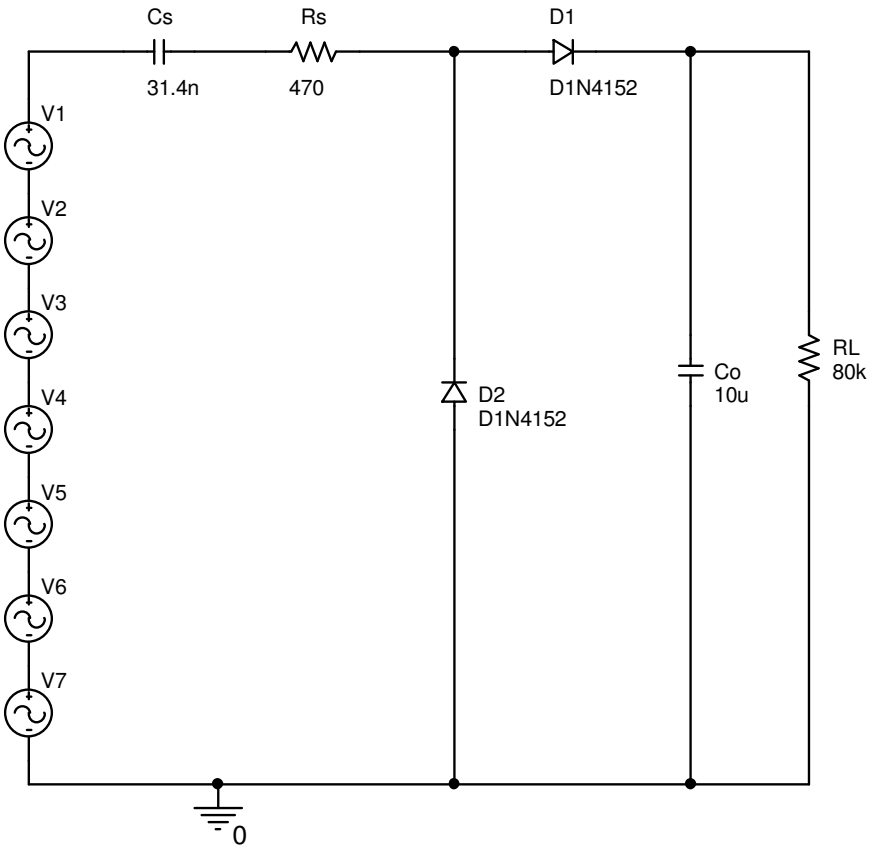
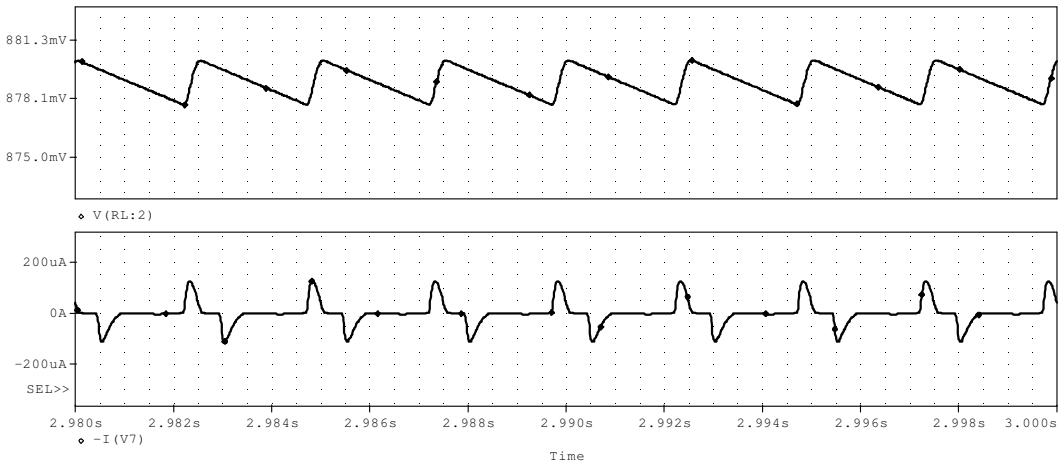
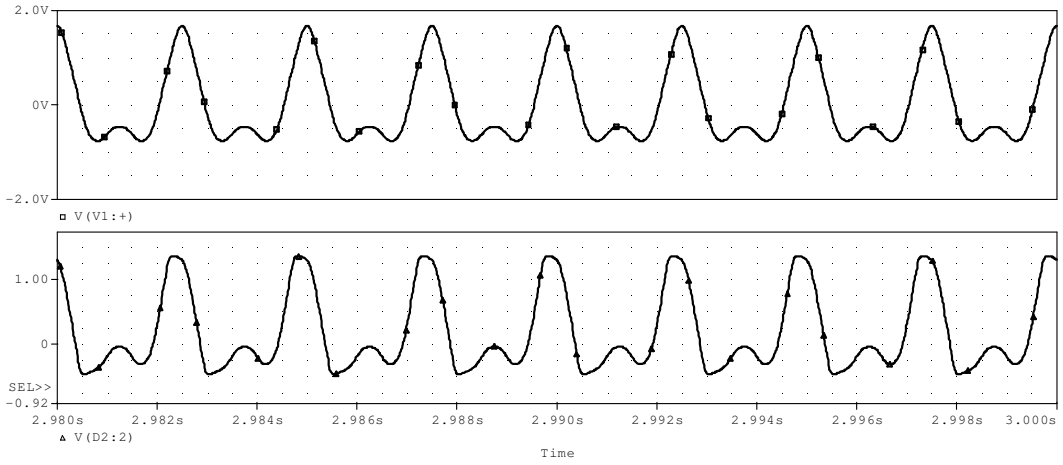


Fig. 3.11. Schematic for PSpice simulation of scheme II rectifier.



(a) Upper: output voltage waveform for an 80kΩ resistive load
Bottom: input current waveform for an 80kΩ resistive load



(b) Upper: PZT model terminal voltage waveform during no load
Bottom: PZT model terminal voltage waveform for an 80kΩ resistive load

Fig. 3.12. Scheme II waveforms from PSpice simulation.

Table 3.3 Scheme II simulation results.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.48	7.68
45	0.633	8.9
52.4	0.696	9.24
63.2	0.776	9.53
67.2	0.802	9.57
70.6	0.824	9.62
80	0.878	9.64
85	0.905	9.64
88.5	0.922	9.61
92	0.939	9.58
97	0.962	9.54
102	0.984	9.49
110	1.016	9.38
129.4	1.084	9.08
139.4	1.114	8.9
154.4	1.154	8.63
184.1	1.22	8.08
196.1	1.242	7.87

3.2.3 Scheme III Simulation Results

The PSpice schematic for scheme III rectifier is shown in Fig. 3.13. Fig. 3.14 shows some typical simulation waveforms for scheme III. Table 3.4 shows scheme III simulation results. From Table 3.4, we can see that the maximum power of 17.73μW is extracted for an 80kΩ resistive load.

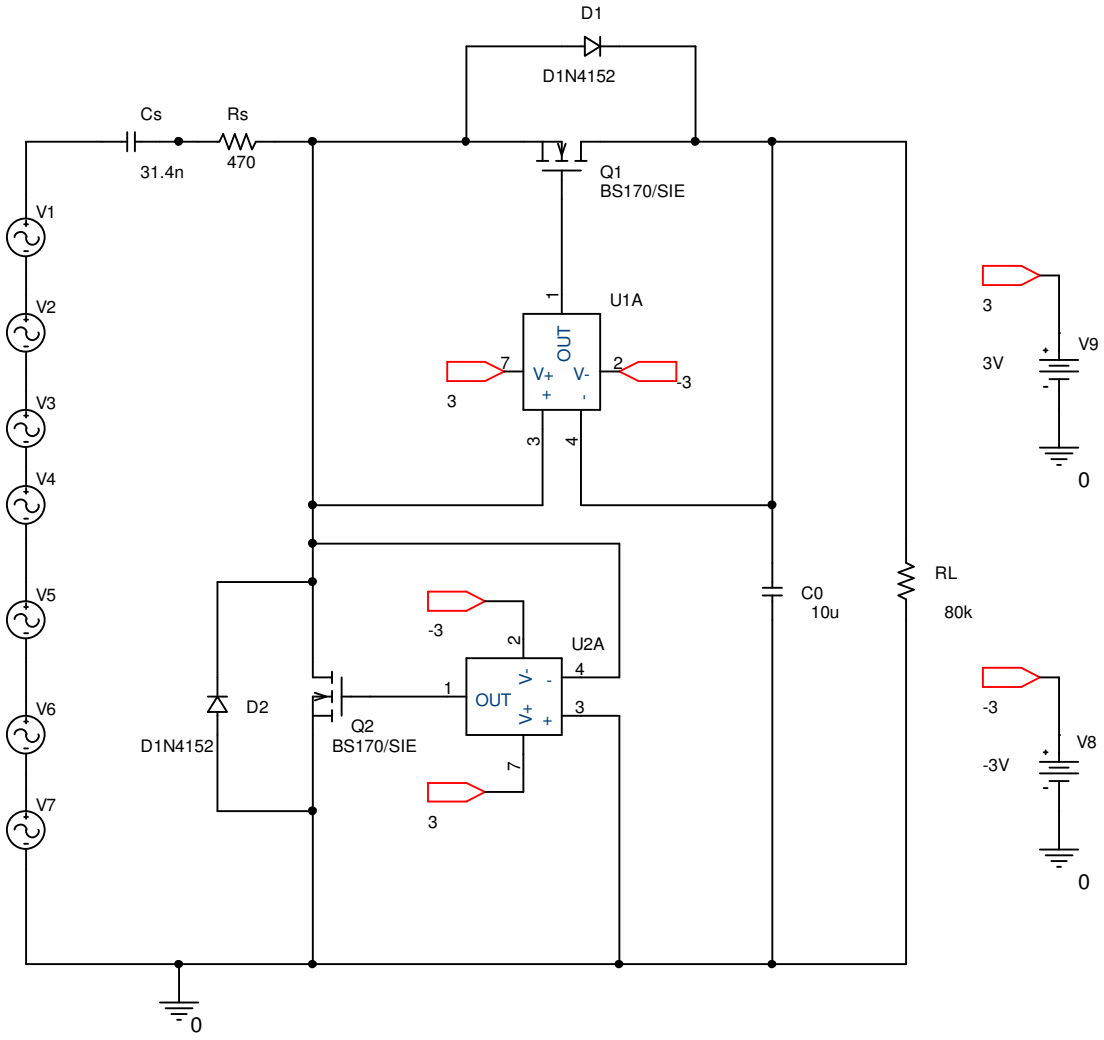
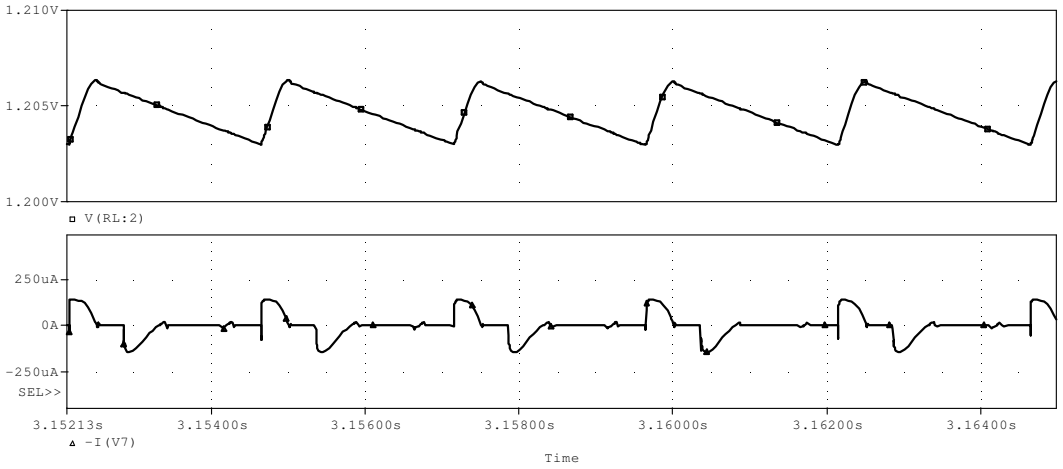
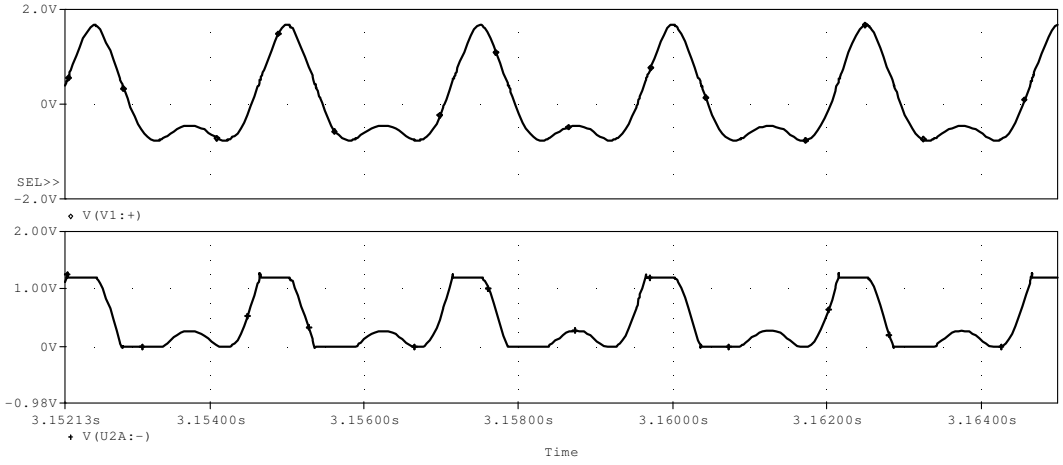


Fig. 3.13. Schematic for PSpice simulation of scheme III rectifier.



(a) Upper: output voltage waveform for an 80kΩ resistive load
Bottom: input current waveform for an 80kΩ resistive load



(b) Upper: PZT model terminal voltage waveform during no load
Bottom: PZT model terminal voltage waveform for an 80kΩ resistive load

Fig. 3.14. Scheme III waveforms from PSpice simulation.

Table 3.4 Scheme III simulation results.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.65	14.08
45	0.858	16.36
52.4	0.944	17
63.2	1.053	17.54
67.2	1.089	17.65
70.6	1.118	17.7
80	1.191	17.73
85	1.225	17.65
88.5	1.249	17.63
92	1.273	17.61
97	1.306	17.58
102	1.335	17.47
110	1.379	17.29
129.4	1.47	16.7
139.4	1.51	16.36
154.4	1.565	15.86
184.1	1.654	14.86
196.1	1.685	14.48

The simulation results of scheme I to scheme III rectifiers are plotted in Fig. 3.15. The PSpice simulation shows that the maximum extracted power with scheme II and scheme III are 225% and 412%, respectively, of that with scheme I. Fig. 3.15 clearly illustrates the superiority of the synchronous rectifier.

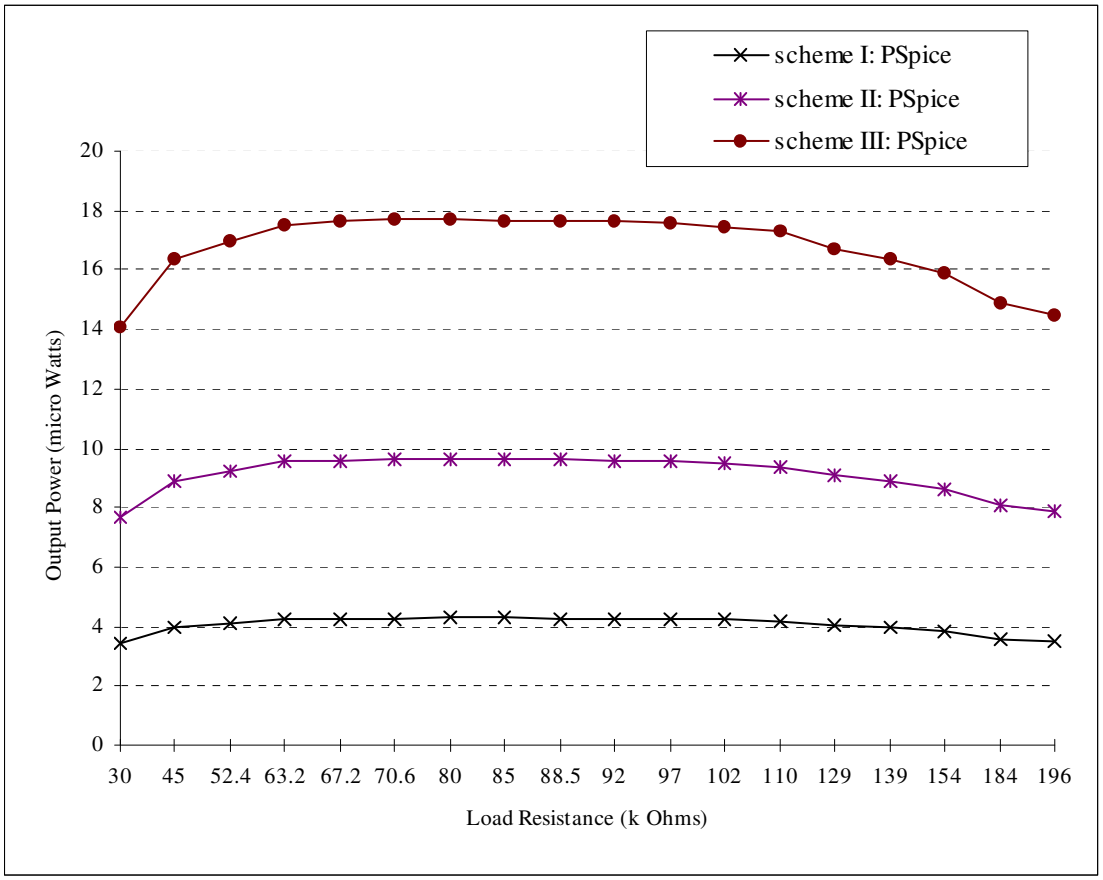


Fig. 3.15. Comparisons of the simulation results of scheme I to scheme III rectifiers.

3.3 Simulation Results for the Regulator Stage

In this section, a 200mW 5V/1.2V step-down charge pump based on the proposed interleaved discharge (ID) method is designed and simulated. In order to show the effectiveness of the ID method, a charge pump based on a conventional control method is first simulated, with the schematic shown in Fig. 3.16, and the simulation waveforms in Fig. 3.17. The simulation results are shown in Table 3.5.

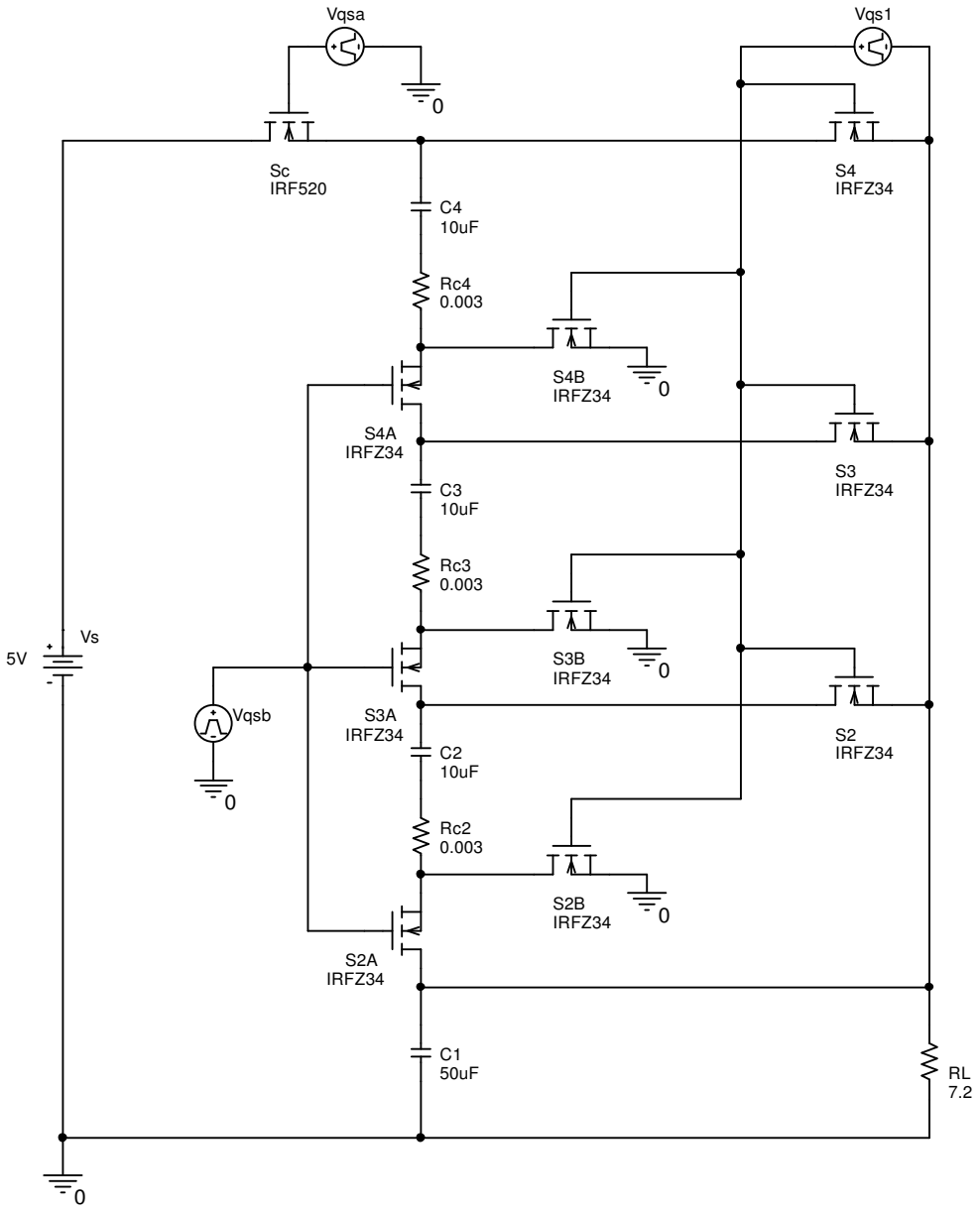


Fig. 3.16. Schematic for PSpice simulation of the 200mW 5V/1.2V charge pump based on a conventional control method.

(a)

(b)

(c)

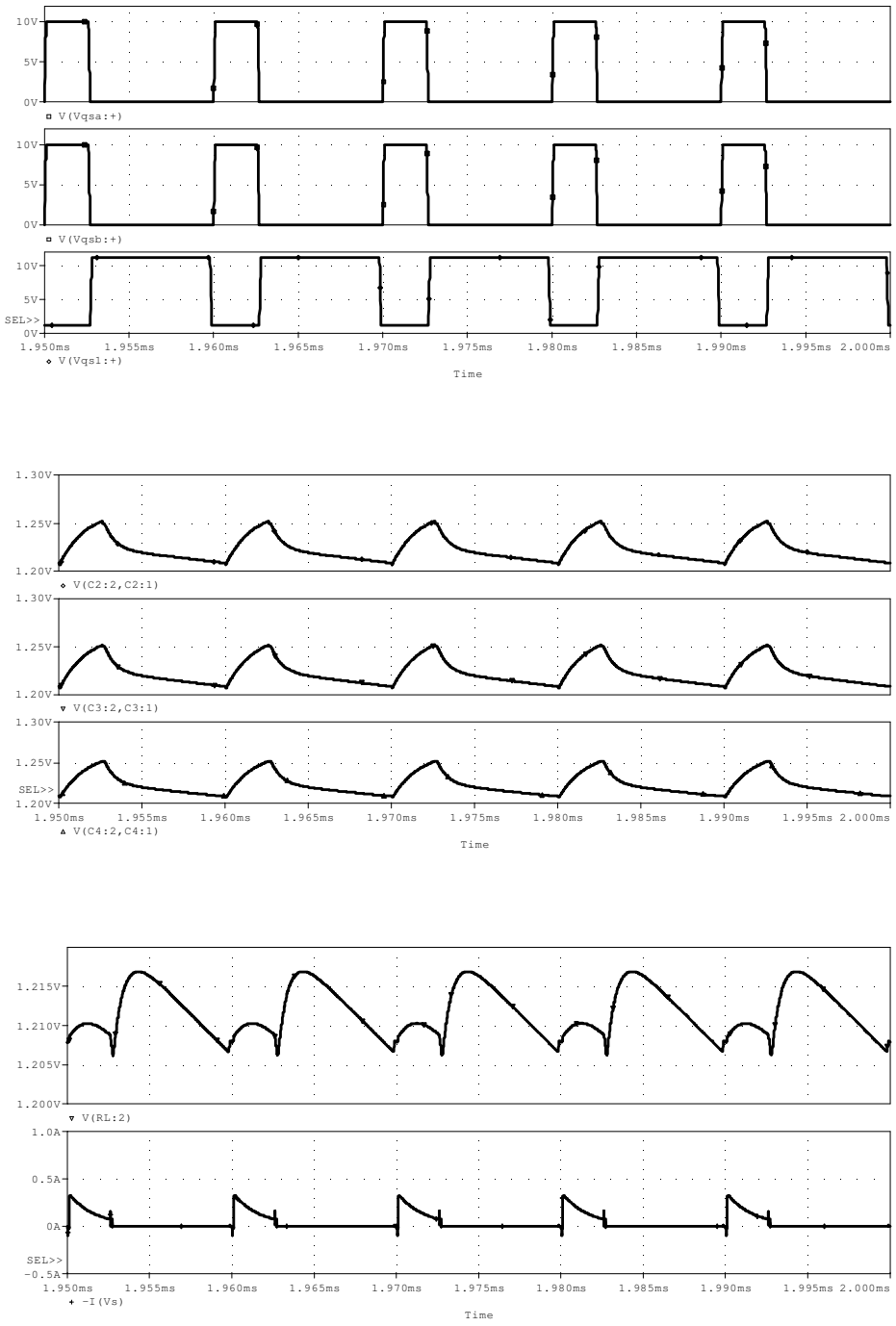


Fig. 3.17. Simulation waveforms of the 200mW 5V/1.2V charge pump based on a conventional control method.
(a) switch driving signals, (b) voltages across capacitors C_2 to C_4 (upper to bottom), and (c) output voltage (upper) and input current (bottom)

Schematic for PSpice simulation of the 200mW 5V/1.2V ID-based charge pump is shown in Fig. 3.18. Fig. 3.19 shows the simulation waveforms. The simulation results are also listed in Table 3.5.

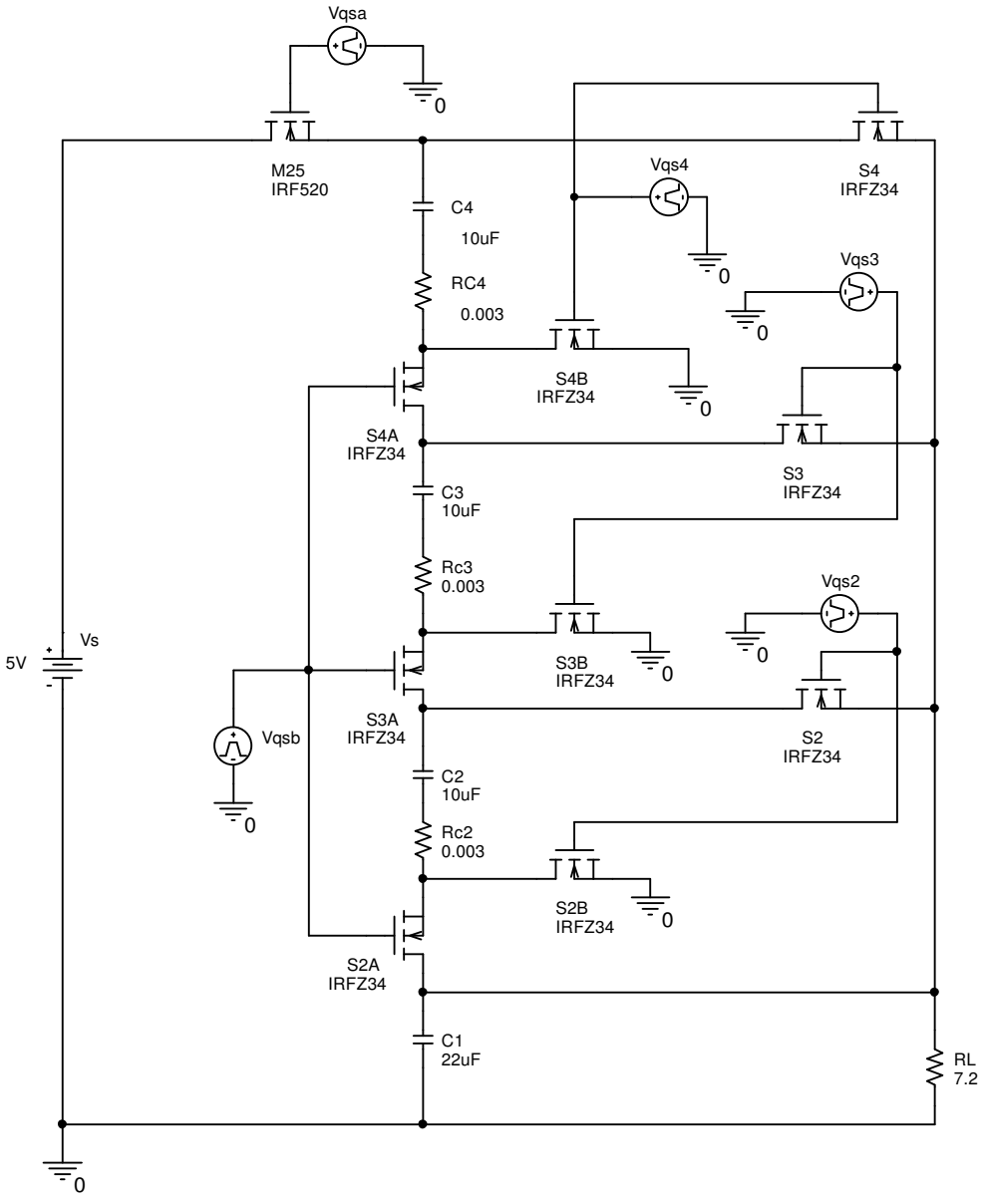


Fig. 3.18. Schematic for PSpice simulation of the 200mW 5V/1.2V charge pump based on the proposed ID method.

(a)

(b)

(c)

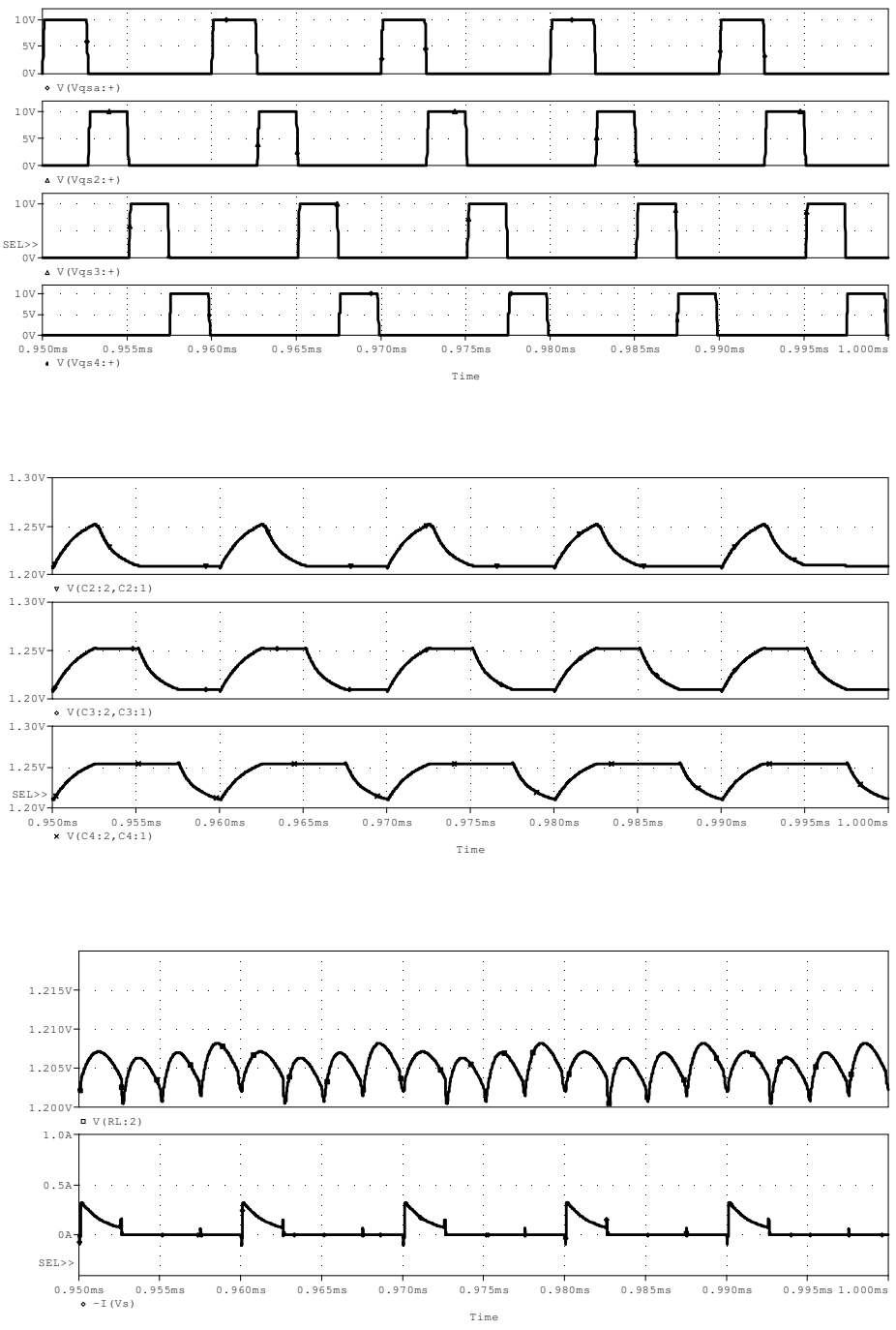


Fig. 3.19. Simulation waveforms of the 200mW 5V/1.2V charge pump based on ID method.
(a) switch driving signals, (b) voltages across capacitors C_2 to C_4 (upper to bottom), and (c) output voltage (upper) and input current (bottom)

Table 3.5 Comparisons of the simulation results of the 200mW, 5V/1.2V charge pump.

	Average Output voltage (V)	Average Input current (mA)	Efficiency (%)	Ripple (mV)
Conventional (C_o=50μF)	1.2117	43.82	93.1	10.7
Proposed (C_o=50μF)	1.2066	43.78	92.4	3.4
Proposed (C_o=22μF)	1.2054	43.8	92.2	7.7

From Table 3.5, it can be noticed that when the output filter capacitance is 50uF, the output ripple of the proposed ID method is only 3.4mV. If we do not need such low output ripple, e.g., 1% ripple is good enough, then we can use the proposed ID method to reduce the filter capacitance. The simulation results are also shown in Table 3.5. It shows that with a 22μF filter capacitance, the output ripple is better than 1%. The ID method could also be used to reduce the charge pump switching frequency so that the converter efficiency can be improved.

All the simulation netlists are given in Appendix A.

3.4 Summary

In this chapter, the proposed PCC was simulated. In order to facilitate the PZT simulation in PSpice, a simplified PZT model was developed. The output voltage spectrum of the PZT was analyzed with Fast Fourier Transform (FFT) so that the PSpice PZT model can generate the same waveforms as the real PZT membranes. After that, three possible rectifier topologies were simulated with PSpice. A 5V/1.2V, 200mW, 1% output ripple charge pump was also simulated. Simulations show that the

interleaved discharge method takes full advantage of the step-down charge pump structure, and leads to some flexibilities in the design of step-down charge pumps.

4 EXPERIMENTAL SETUPS

4.1 Proof-Of –Concept Demonstration

For the purpose of proof-of-concept demonstration, a totally passive, as required by DARPA, PCC has been designed, as shown in Fig. 4.1. Diode D_1 rectifies the ac output of the P^3 engine. The 4-stage charge pump is operated manually through four toggle switches. The load is an analog wristwatch. At the beginning of the project, a PVDF membrane served as the piezoelectric generator.

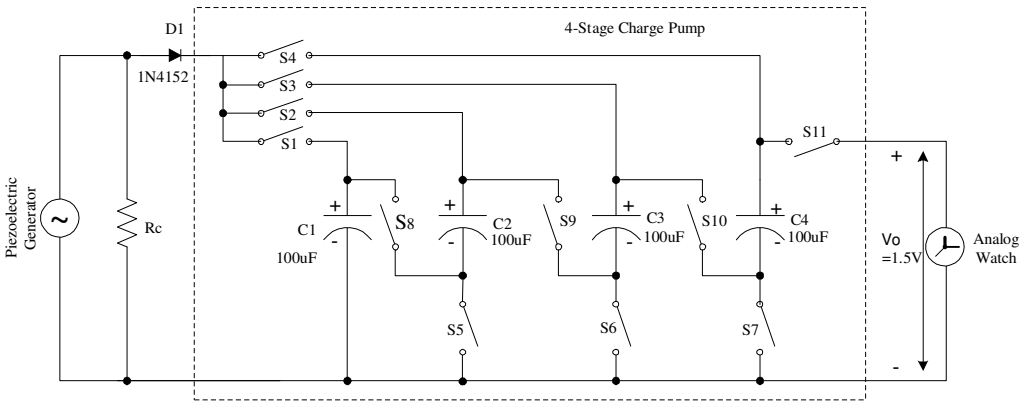


Fig. 4.1. Circuit for the proof-of-concept demonstration.

The circuit in Fig. 4.1 was built on a proto board. The layout of the board is shown in Fig. 4.2. Switches S_1, S_2, S_8, and S_9 are integrated in the dual pole dual throw (DPDT) toggle switch TS_1. S_3, S_4, S_{10}, and S_{11} are integrated in the DPDT toggle switch TS_2. S_5 and S_6 take the DPDT toggle switch TS_3. S_7 is in the single pole single throw (SPST) toggle switch TS_4. The operation instruction of the demonstration circuit is shown in the Appendix B.

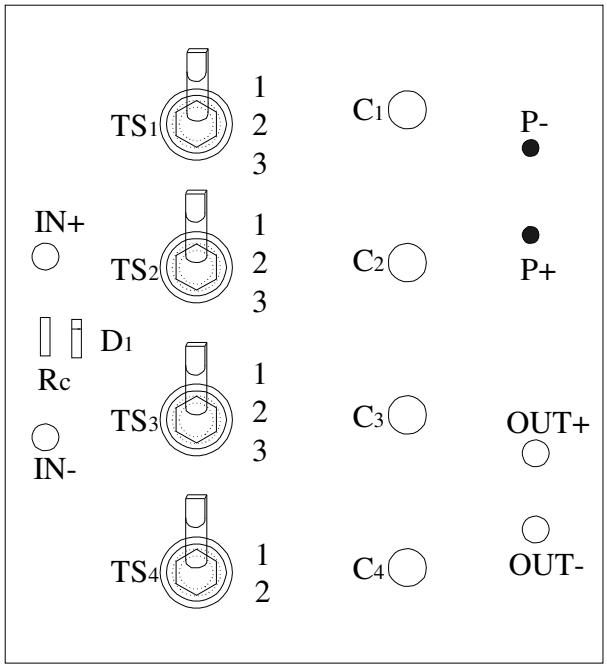


Fig. 4.2. Layout of the proof-of-concept demonstration circuit.

4.2 Bulge Tester

The schematic for the bulge tester experimental setup is shown in Fig. 4.3. It is based on the bulge tester and the PZT membranes provided by researchers at Washington State University. The bulge tester is used to simulate the action of the micro heat engine that drives the PZT membranes. PZT membranes of different sizes are fabricated on a wafer. An actuator in the bulge tester provides the periodic mechanical excitation, through the DI water inside the aluminum pressure chamber, to the PZT membrane, which generates an ac voltage. The PCC then converts this ac voltage into the regulated dc voltage required by the load. The actuator is driven by a sine wave input in the range of -20Vac~120Vac, provided by a 120kVA programmable source, in the Motor Systems Resource Facility (MSRF) at Oregon State University. A dc power supply is connected in series to the programmable source to provide the necessary offset. Fig. 4.4 (a) and (b) shows the

photos of the bulge tester and the wafer within its holder, respectively. Fig. 4.4 (c) is the photo of the 120kVA programmable source in the MSRF. Fig. 4.5 illustrates the cross section of the bulge tester.

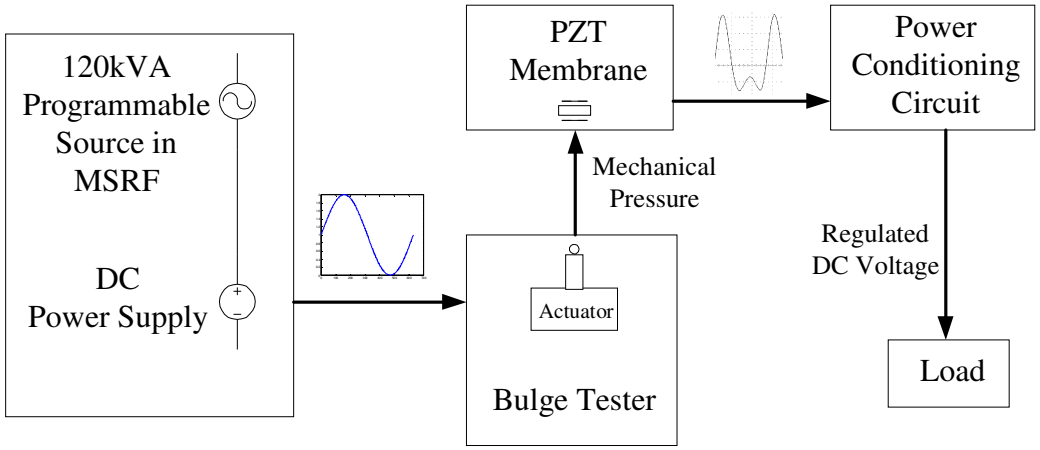
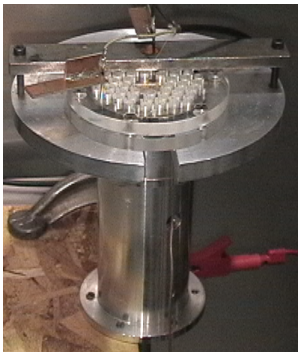
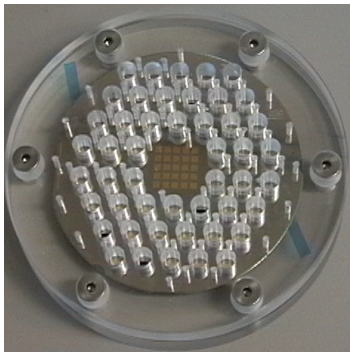


Fig. 4.3. Experimental setup of the bulge tester.



(a)



(b)

(c)

Fig. 4.4. Photos of the experimental setup
(a) Bulge tester, (b) Wafer and its holder, and (c) the 120kVA programmable source in the MSRF.

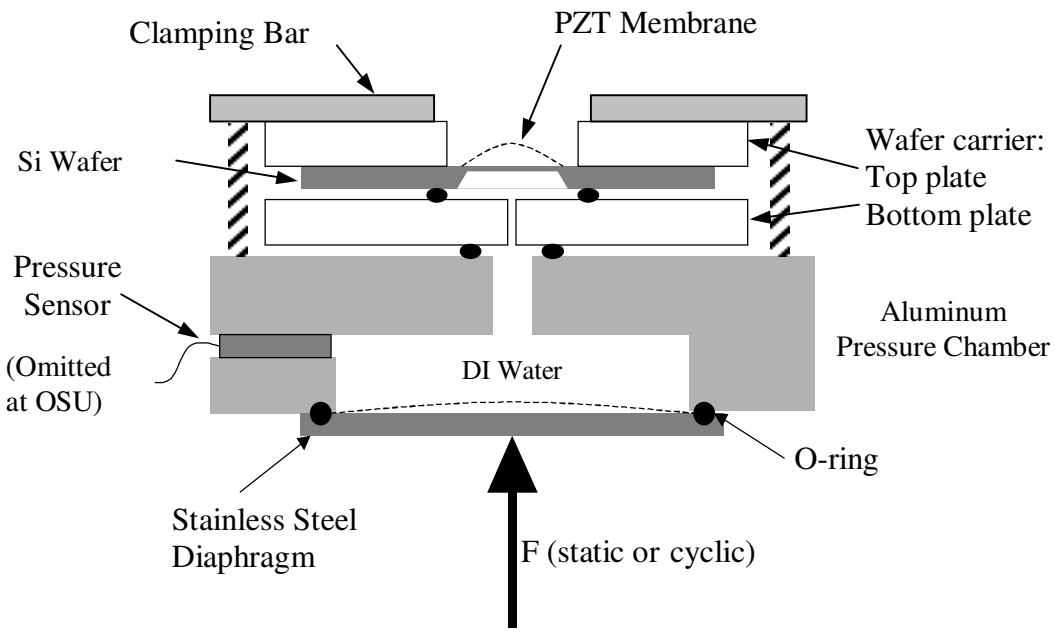


Fig. 4.5. Cross section of the bulge tester [14].

5 EXPERIMENTAL RESULTS AND DISCUSSIONS

5.1 Test Results for the Proof-Of-Concept Demonstration

The circuit for the proof-of-concept demonstration has already been shown in Fig. 4.1. It consists of a rectifier and a 4-stage charge pump. The 4-stage charge pump has two operation stages: first, aluminum electrolytic capacitors C_1~C_4 are arranged in parallel, and charged to 0.39V in about 2 minutes with no load; second, the four capacitors are connected in series to get 1.56V dc voltage, which runs the wristwatch for 5 seconds. Although the delivered power is very low, this simple demonstration does show that the entire system works. The resistor R_C helps to extract additional power from the piezoelectric membrane. Fig. 5.1 shows the capacitor terminal voltage as a function of the charging time at different R_C values. Four 100μF capacitors were charged to 1.0Vdc in parallel. Different R_C values were tested. The peak-to-peak output voltage of the piezoelectric generator is 2.09V. When R_C=45kΩ, the charging time is minimized, about 8.5 times shorter than the case without R_C.

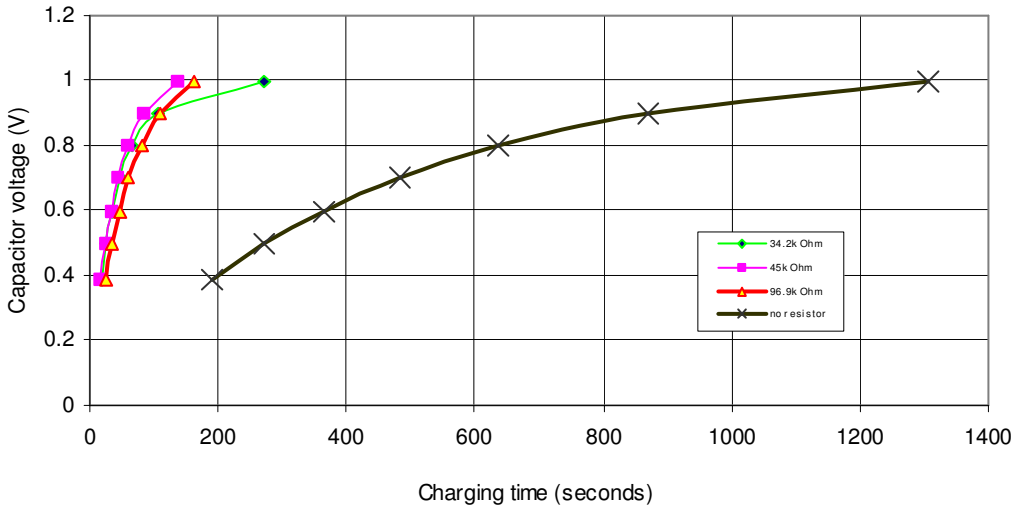


Fig. 5.1. Charging time comparison.

5.2 Test Results for the Bulge Tester

In this section, the characterization results of all the PZT membranes are given. A 21Vdc voltage was applied to the terminal leads of each PZT membrane to activate it. This process is called poling. Then, test results of the rectifier stage with the bulge tester are presented.

5.2.1 PZT Membrane Characterization

All the PZT membranes on the wafer were numbered according to Fig. 5.2. The impedances of the each available membrane, before and after poling, are measured with an HP4284A Precision LCR Meter. The peak-peak output voltages of each available membrane are also measured during tests of the bulge tester. The results are recorded in Table 5.1. Note that membrane H3 is the prototype of the proposed simplified PZT model in Chapter 3.

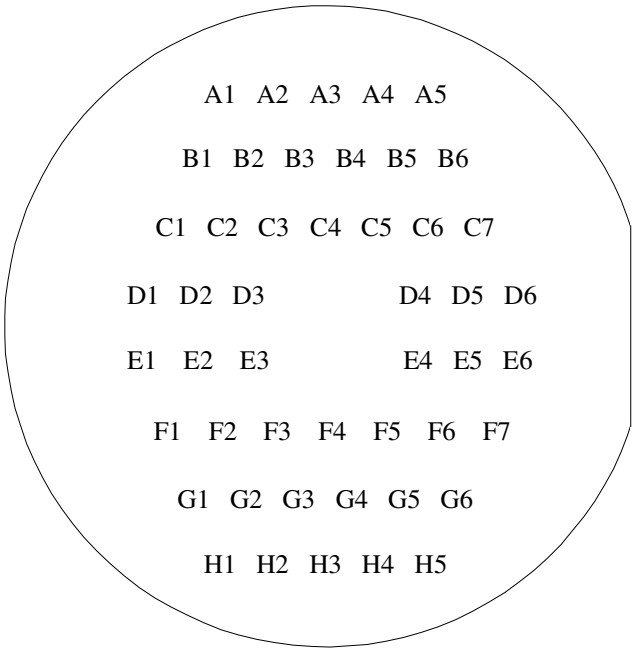


Fig. 5.2. PZT membrane numbering.

Table 5.1 PZT membrane characterization results.

Membrane #	Before poling		After poling		PZT output (Vpp)
	Capacitance Cs (nF)	Resistance Rs (Ohm)	Capacitance Cs (nF)	Resistance Rs (Ohm)	
A1	32.0	411	30.7	500	1.9
A2	33.0	376	31.7	455	2.4
A3	X*	X	X	X	X
A4	X	X	X	X	X
A5	33.2	367	31.6	439	1.7
B1	32	415	30.8	500	2.2
B2	X	X	X	X	X
B3	34.6	430	32.1	440	2.3
B4	X	X	X	X	X
B5	33.38	384	31.65	445	3
B6	32.7	376	31.7	434	X
C1	31.4	401	30.5	484	2.7
C2	33.6	409	31.7	466	2.5
C3	X	X	X	X	X
C4	32.3	387	30.2	435	2.3
C5	32.1	368	31	450	2.0
C6	32.9	373	31.6	439	2.4
C7	33	375	31.6	436	2.4
D1	30.9	415	29.6	500	2.0
D2	32.8	416	31	475	2.3
D3	/**	/	27.5	300	2.2
D4	31.8	388	30	450	3.2
D5	33	385	31.6	435	2.7
D6	33.2	373	31.8	440	3.0
E1	30.8	410	29.8	512	1.8
E2	32.4	415	30.6	465	2.5
E3	/	/	27	287	2.2
E4	29	405	27.4	330	2.2
E5	X	X	X	X	X
E6	33.3	386	31.8	440	2.3
F1	30	404	29.2	527	2.0
F2	X	X	X	X	X
F3	32.6	369	31.4	453	2.1
F4	32.1	380	30.6	446	2.4
F5	32.5	370	31.2	453	2.6
F6	33.4	400	31.6	433	2.7

Table 5.1 PZT membrane characterization results (continued).

Membrane #	Before poling		After poling		PZT output (Vpp)
	Capacitance Cs (nF)	Resistance Rs (Ohm)	Capacitance Cs (nF)	Resistance Rs (Ohm)	
F7	33.5	379	32	438	3.2
G1	30.8	410	29.8	510	1.9
G2	32.4	387	31.2	470	2.4
G3	X	X	X	X	X
G4	33.9	380	29.7	430	1.2
G5	34.5	392	31.9	438	X
G6	X	X	X	X	X
H1	X	X	X	X	X
H2	32.3	406	28.6	430	2.3
H3	32.7	384	31.4	470	2.5
H4	33.8	410	31.5	454	2.0
H5	34.2	377	32.3	430	2.2

Notes:

* The membranes marked with ‘X’ were bad or broken before characterization.

** The parameters marked with ‘/’ were unavailable, because the corresponding PZT membranes were poled at Washington State University.

5.2.2 Scheme I Test Results

The scheme I rectifier as shown in Fig. 2.3 was tested with the bulge tester. The PZT membranes’ resonant frequency is about 400Hz. The test results of scheme I rectifier with the bulge tester are given in Table 5.2. As can be seen, a maximum power of 3.7μW was extracted under an 80kΩ resistive load.

Table 5.2 Scheme I test results with the bulge tester.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.298	2.96
45	0.395	3.47
52.4	0.416	3.3
63.2	0.466	3.44
67.2	0.485	3.5
70.6	0.502	3.57
80	0.544	3.7
85	0.558	3.66
88.5	0.568	3.65
92	0.575	3.59
97	0.588	3.56
102	0.596	3.48
110	0.617	3.46
129.4	0.658	3.35
139.4	0.681	3.33
154.4	0.711	3.27
184.1	0.752	3.07
196.1	0.762	2.96

5.2.3 Scheme II Test Results

The scheme II rectifier as shown in Fig. 2.5 was tested with the bulge tester. The test results are given in Table 5.3. A maximum power of 7.86μW was extracted for an 80kΩ resistive load.

Table 5.3 Scheme II test results with the bulge tester.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.425	6.02
45	0.562	7.02
52.4	0.624	7.43
63.2	0.692	7.58
67.2	0.723	7.78
70.6	0.733	7.61
80	0.793	7.86
85	0.813	7.78
88.5	0.828	7.75
92	0.839	7.65
97	0.857	7.57
102	0.894	7.84
110	0.929	7.85
129.4	1	7.73
139.4	1.035	7.68
154.4	1.079	7.54
184.1	1.09	6.45
196.1	1.133	6.55

5.2.4 Scheme III Test Results

The scheme III rectifier as shown in Fig. 2.6 was tested with the bulge tester. The test results of scheme III rectifier with bulge tester are given in Table 5.4. A maximum power of 18.83μW was extracted for a 70.6kΩ resistive load.

Table 5.4 Scheme III test results with bulge tester.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.662	14.61
45	0.858	16.36
52.4	0.95	17.22
63.2	1.043	17.21
67.2	1.094	17.81
70.6	1.153	18.83
80	1.198	17.94
85	1.212	17.28
88.5	1.248	17.6
92	1.294	18.2
97	1.322	18.02
102	1.328	17.29
110	1.418	18.28
129.4	1.459	16.45
139.4	1.518	16.53
154.4	1.558	15.72
184.1	1.623	14.31
196.1	1.642	13.75

Fig. 5.3 shows a typical PZT output voltage waveform during no load. Fig. 5.4 (a) and (b) shows the scheme III output voltage and PZT terminal voltage waveforms, respectively, for a 70.6kΩ resistive load.

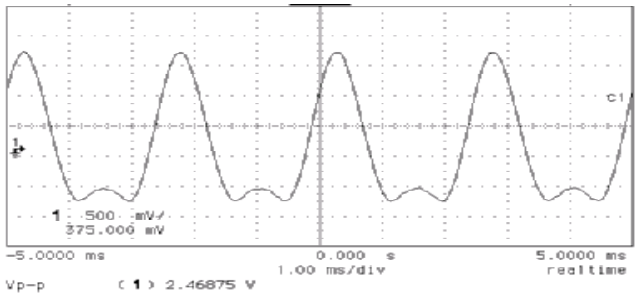
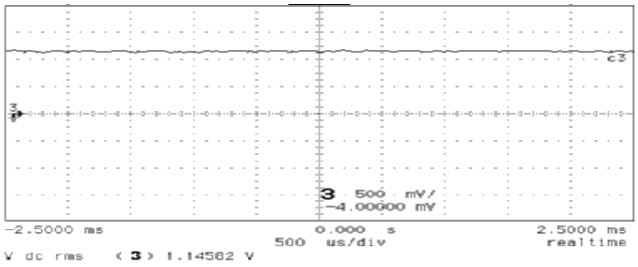
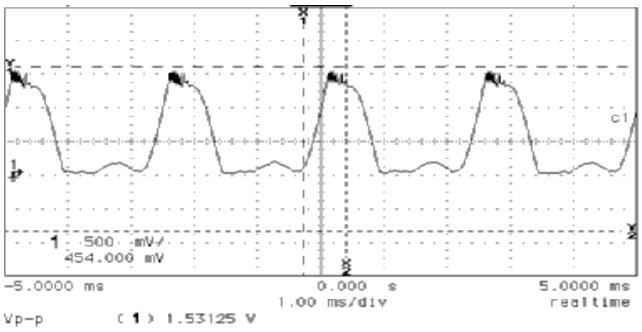


Fig. 5.3. PZT output voltage waveform during no load.



(a) Output voltage waveform for a 70.6kΩ resistive load



(b) PZT terminal voltage waveform for a 70.6kΩ resistive load

Fig. 5.4. Waveforms of scheme III rectifier with bulge tester.

5.3 Discussions

The extracted powers at different loads for the three rectification schemes are shown in Fig. 5.5. It can be noted that scheme I can extract a maximum power of 3.7μW for an 80kΩ load. The maximum power extracted by scheme II and scheme III is 212% (for an 80kΩ load) and 508% (for a 70.6kΩ load) of that of scheme I, respectively. Also, compared with Fig. 3.11, the test results of the bulge tester coincide very well with the PSpice simulation results. Hence, the simplified model for the piezoelectric generator used in the PSpice simulation is experimentally verified.

It should be pointed out that there was no pressure sensor in the bulge tester built for OSU (refer to Fig. 4.5.). The initial pressure of the DI water inside the chamber was mainly dependent on how tight the clamping bars were fastened, which on the other hand could only be dependent on the operator's experience. If the clamping bars were fastened too tight, the silicon wafer would be broken; if the clamping bars were not fastened tight enough, there might be DI water leakage under the PZT membrane under test, which would lead to unstable PZT output voltages. In fact, the second scenario happened often during the test, and it gave rise to the fluctuations in the output power curve of scheme III, as shown in Fig. 5.5. This is also the reason why the maximum power point of scheme III (70.6kΩ load) was different from the normal maximum power point of an 80kΩ load.

For scheme III, the power consumption of the comparators should not present a problem, since off-the-shelf nanopower comparators with a supply current of only 0.38μA (3V supply voltage, at 25°C) are currently available [46]. Considering this power consumption (2.28μW, two comparators), the extracted power is still 447% of that of scheme I. In the future, with the PCC being integrated on a single chip, the comparator power consumption will be further decreased. Also, with more P^3 unit cells working together, the output power will be increased, and the comparator consumption becomes more negligible. A low power rechargeable

"button-cell" battery can start up the circuit. During normal operation of the MPG, the battery will be trickle charged. In fact, scheme III has another potential advantage. A simple study on Fig. 3.6 shows that the body diodes of the two MOSFETs have actually formed a diode-diode pair rectifier, i.e., scheme II. If there are no power supplies for the comparators, then scheme III will be degraded into scheme II, and there will still be dc output voltage. This voltage can then be regulated with on-chip charge pumps to drive the comparators, and scheme III will be activated, i.e., the circuit can be self-started. Therefore, it is possible to develop a totally passive PCC with scheme III.

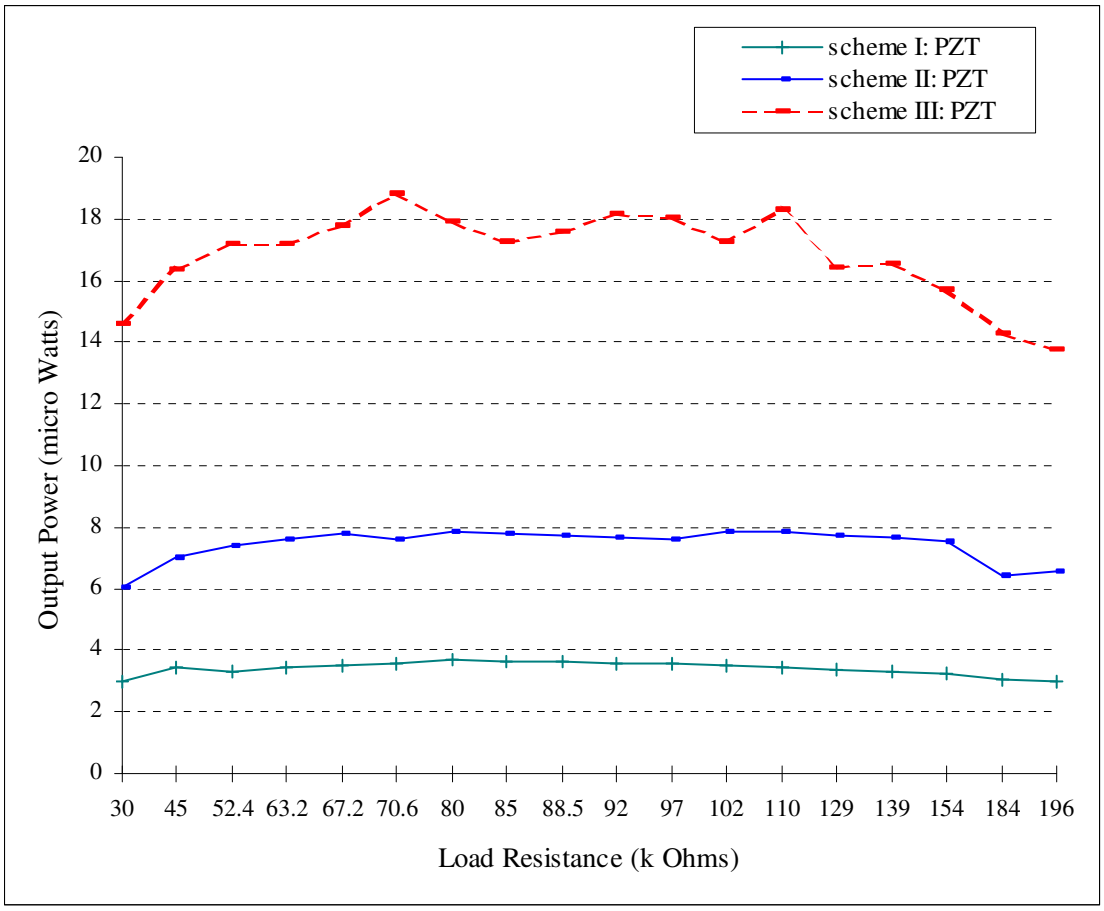


Fig. 5.5. Comparisons of scheme I to scheme III rectifiers with bulge tester.

5.4 Summary

In this chapter, the characterization results of all the PZT membranes were given. Then, the experimental results for the proof-of-concept demonstration and the bulge tester were presented. Scheme I can extract a maximum power of 3.7μW with an 80kΩ load. The maximum power extracted by scheme II and scheme III is 212% and 508% of that of scheme I, respectively. Test results of the bulge tester coincide very well with the PSpice simulation results. Hence, the simplified model for the piezoelectric generator used in the PSpice simulation is experimentally verified. The structure of scheme III makes it possible to develop a totally passive PCC.

6 ARBITRARY WAVEFORM GENERATOR REPRESENTATION (AWGR) OF THE PZT MEMBRANE

Since the power of a single generator cell is only on the level of microwatts, in order to achieve higher power, it is necessary to connect many cells in series or in parallel according to the load requirements. At the current stage of the project, it is impractical to build several bulge testers for the PCC experiments. An alternative to the bulge tester is to develop a representative system with an arbitrary waveform generator and the necessary interfacing circuits.

6.1 AWGR Setup

An arbitrary waveform generator representation (AWGR) of a generator cell has been developed, as shown in Fig. 6.1.

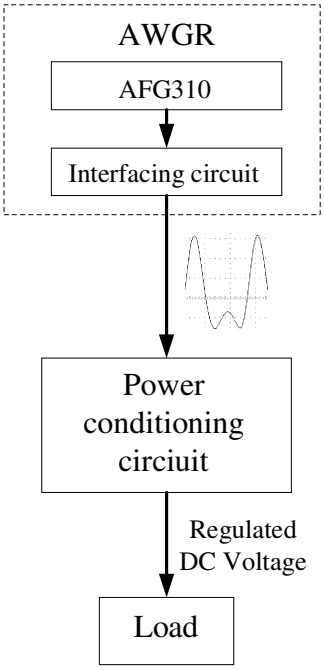


Fig. 6.1. Block diagram of the AWGR.

The interfacing circuit in Fig. 6.1 was obtained with the PZT impedance parameters, i.e., the same as those obtained for the simplified PZT model. The actual waveform of a P^3 cell is transferred to the arbitrary function generator AFG310 via a general purpose interface bus (GPIB) cable, as shown in Fig. 6.2.

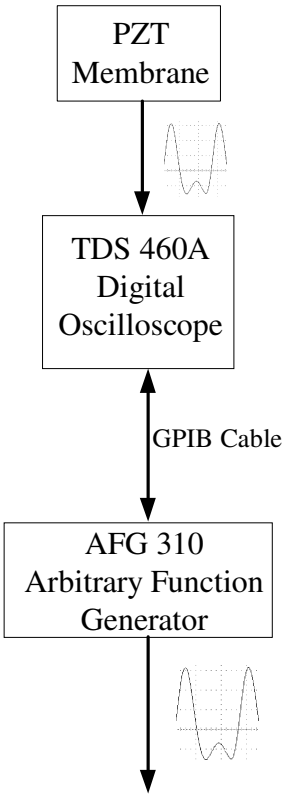


Fig. 6.2. Transferring the PZT output waveform into AFG 310.

6.2 AWGR Test Results

All the three rectifier schemes as discussed in Chapter 2 were studied with the AWGR, and the results are shown in Table 6.1 ~ Table 6.3. Operation instructions for the AWGR are given in Appendix C. For scheme I, the maximum power of 3.84μW was extracted for an 80kΩ resistive load. For scheme II, the maximum power of

7.59μW was extracted for an 80kΩ resistive load. The extracted maximum power of scheme III was 17.18μW for an 88.5kΩ resistive load. Fig. 6.3 compares the PSpice simulation, bulge tester, and AWGR test results. It can be seen that the AWGR test results are very close to that of the bulge tester. Fig. 6.4 shows some waveforms of scheme III for an 80kΩ load.

Table 6.1 Scheme I test results with AWGR.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.302	3.04
45	0.398	3.52
52.4	0.442	3.73
63.2	0.49	3.8
67.2	0.505	3.8
70.6	0.519	3.82
80	0.554	3.84
85	0.57	3.82
88.5	0.582	3.83
92	0.586	3.73
97	0.6	3.72
102	0.621	3.78
110	0.642	3.75
129.4	0.685	3.63
139.4	0.706	3.58
154.4	0.732	3.47
184.1	0.776	3.27
196.1	0.791	3.19

Table 6.2 Scheme II test results with AWGR.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.42	5.88
45	0.557	6.89
52.4	0.616	7.24
63.2	0.685	7.42
67.2	0.709	7.48
70.6	0.728	7.51
80	0.779	7.59
85	0.803	7.59
88.5	0.818	7.56
92	0.834	7.56
97	0.856	7.55
102	0.876	7.52
110	0.907	7.48
129.4	0.966	7.21
139.4	0.995	7.1
154.4	1.034	6.92
184.1	1.095	6.51
196.1	1.117	6.36

Table 6.3 Scheme III test results with AWGR.

Load Resistance (kΩ)	Output Voltage (V)	Output Power (μW)
30	0.639	13.61
45	0.849	16
52.4	0.93	16.51
63.2	1.031	16.82
67.2	1.068	16.97
70.6	1.097	17.05
80	1.171	17.14
85	1.208	17.17
88.5	1.233	17.18
92	1.254	17.09
97	1.286	17.05
102	1.313	16.9
110	1.349	16.54
129.4	1.432	15.85
139.4	1.466	15.42
154.4	1.521	14.98
184.1	1.621	14.27
196.1	1.642	13.75

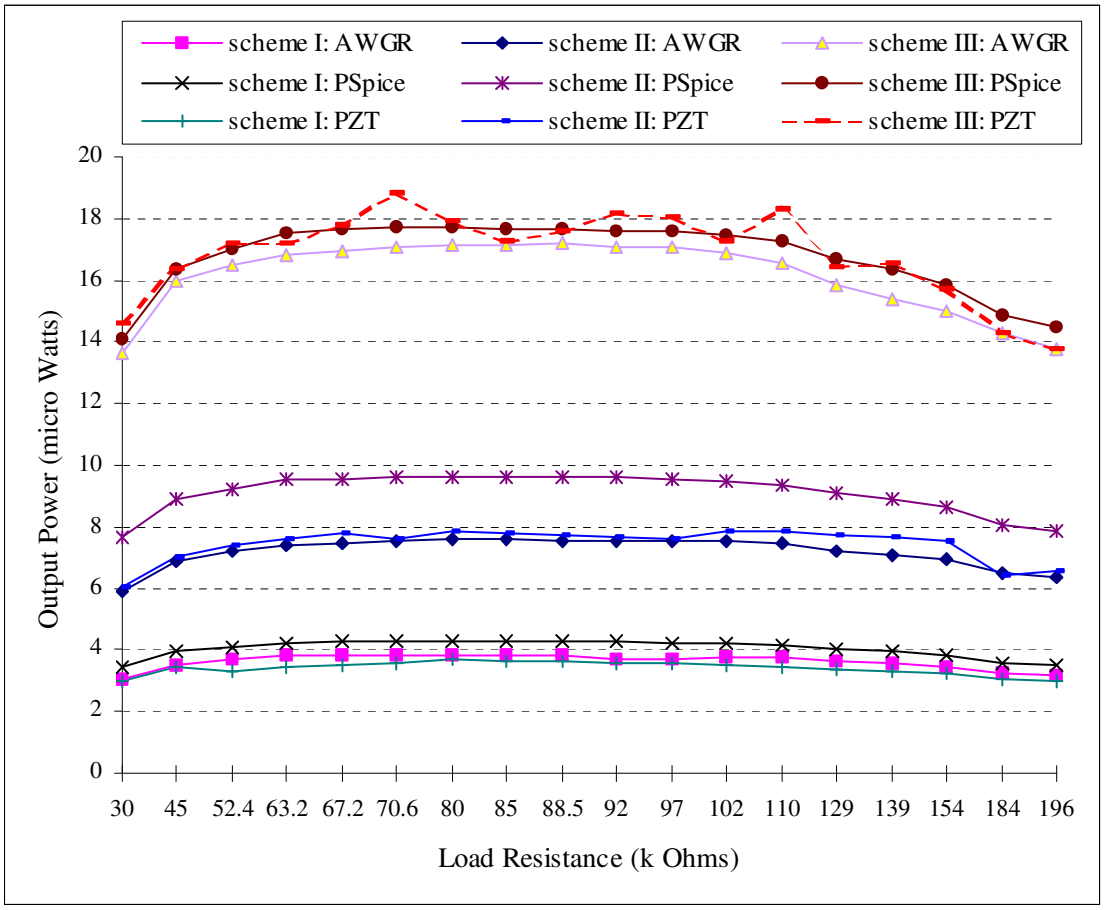


Fig. 6.3. Comparisons of the simulation, bulge tester, and AWGR results.

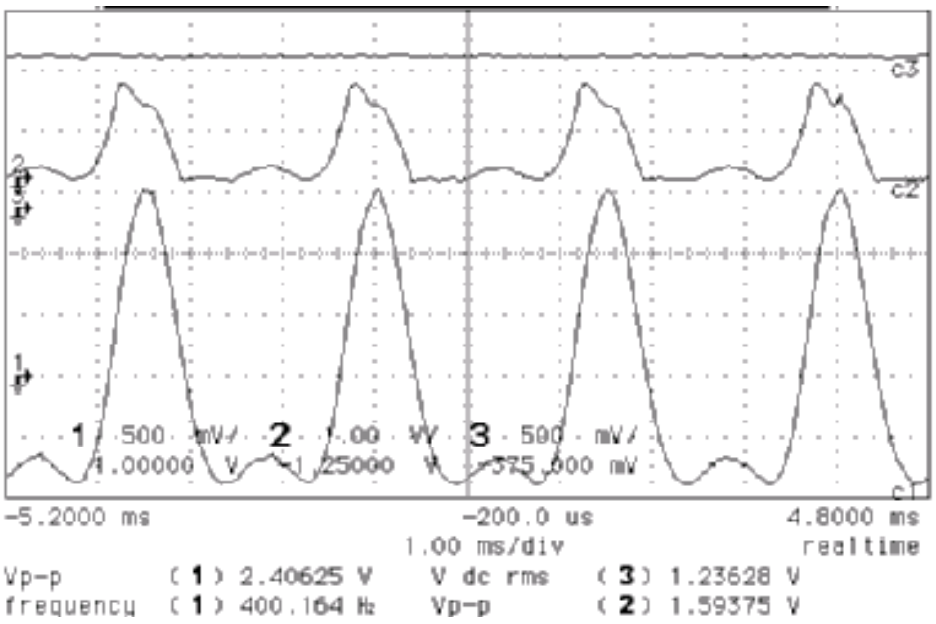


Fig. 6.4. Typical waveforms of scheme III from AWGR test.
Upper: output dc voltage; Middle: PCC input voltage; and Bottom: AWGR no-load output voltage.

6.3 Efficiency Evaluation with the AWGR

During the test of the bulge tester, it is difficult to measure the input current. If we use a large current sensing resistor, it will degrade the PZT output power. If the sensing resistor is too small, we cannot measure the current accurately.

Since the AWGR has already been validated in the above section, we can now take full advantage of its capabilities. Fig. 6.5 illustrates the AWGR being connected to scheme III. From Fig. 6.5 we can easily see that R_S could be utilized to measure the input current to the PCC. Denote the voltage across R_S as V_1, and then the input current to the rectifier is

$$I_{in} = \frac{V_1}{R_S} \tag{6-1}$$

The input and output voltage of the rectifier stage can be readily measured, denoted here as V_{in} and V_0. Therefore, the input power is

$$P_{in} = V_{in} \times I_{in} = \frac{V_{in} \times V_1}{R_S} \tag{6-2}$$

Since the output power is

$$P_{out} = \frac{V_0^2}{R_L} \tag{6-3}$$

Hence, we can easily find the efficiency of the rectifier stage, which is expressed as

$$\eta = \frac{P_{out}}{P_{in}} \tag{6-4}$$

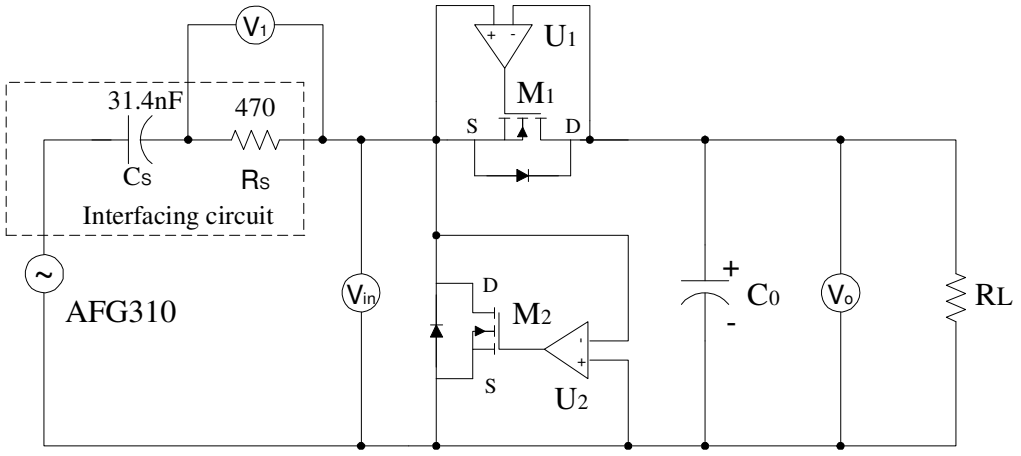


Fig. 6.5. AWGR connected to scheme III.

The efficiencies of scheme I ~ scheme III were evaluated based on the above-mentioned method. For an 80kΩ resistive load, the efficiency of scheme I, II, and III is approximately 34%, 57%, and 92%, respectively. Fig. 6.6 shows the efficiency test results. Fig. 6.7 shows some waveforms for evaluating the efficiency of scheme III. It should be noted that since the base power (input power) for each scheme is quite

different (i.e., the power extraction ability of the three schemes are different), as shown in Table 6.4, a direct efficiency comparison couldn't be made. In the future, after the charge pump is built, the AWGR can be used to estimate the efficiency of the entire PCC.

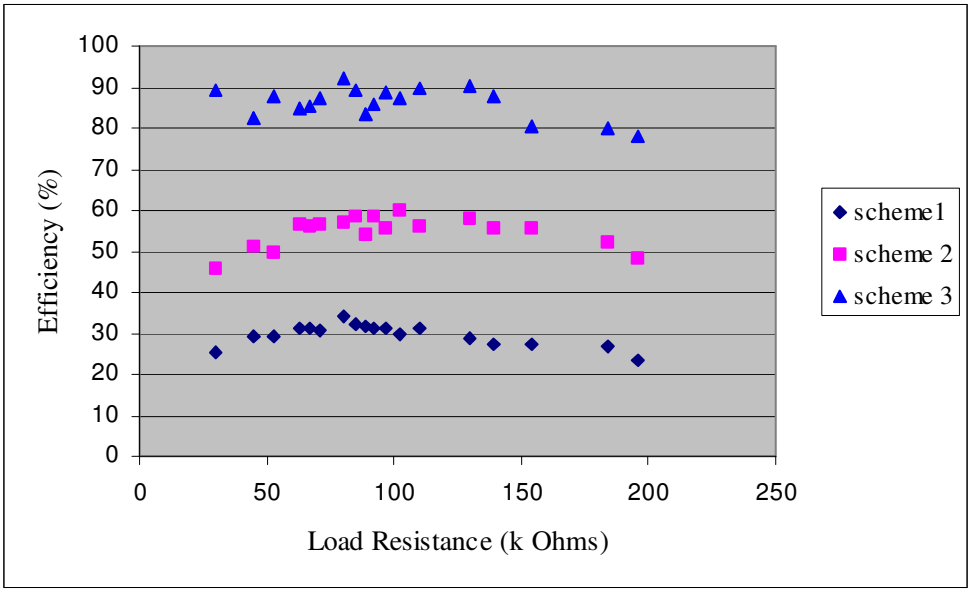


Fig. 6.6 Efficiency test results.

Table 6.4 Efficiency test results for an 80kΩ resistive load.

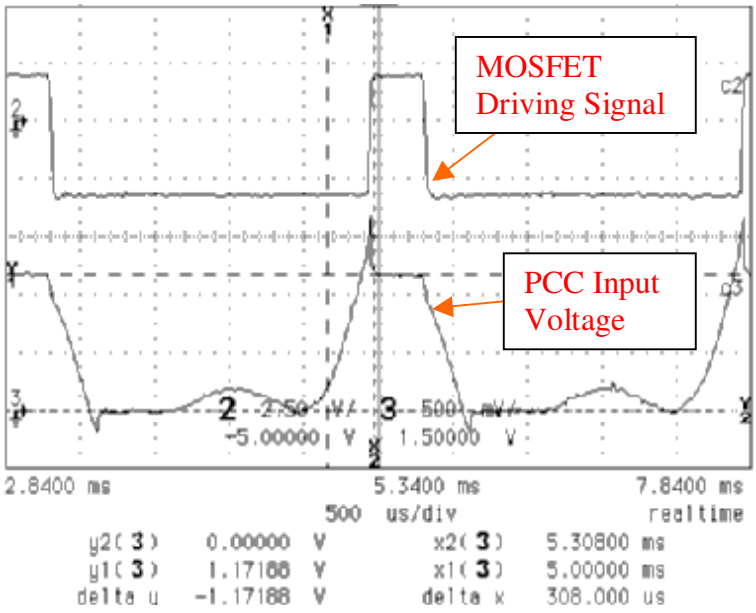
	Input Power (μW)	Output Power (μW)	Efficiency (%)
Scheme I	11.48	3.94	34
Scheme II	13.30	7.56	57
Scheme III	18.70	17.27	92

6.4 Summary

In this chapter, arbitrary waveform generator representation of the PZT membrane is developed. Test results of the three rectifier schemes with AWGR were

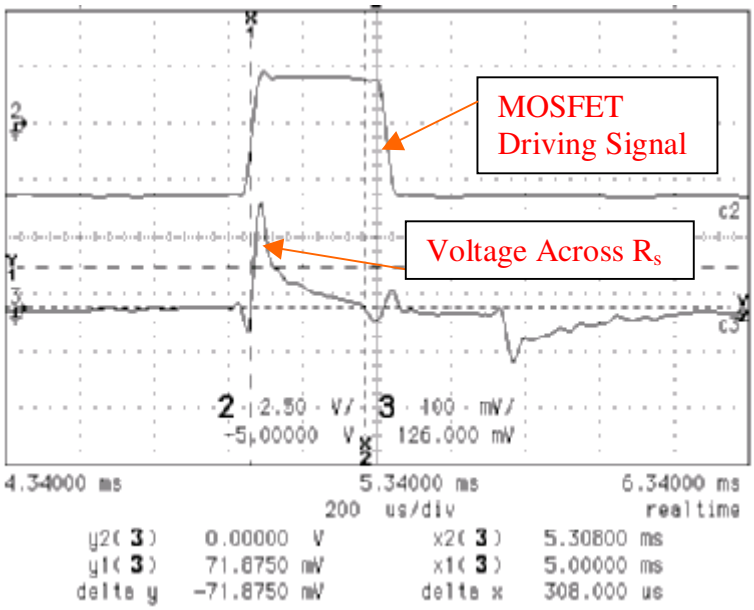
given. The AWGR test results are very close to that of the bulge tester. AWGR was used to evaluate the PCC efficiency. Test results show that the efficiency of scheme III is far more superior to that of scheme I and scheme II.

Compared to the bulge tester, the AWGR is programmable, flexible, more robust, and easier to operate. Therefore, tests can be performed on the AWGR, rather than directly on the bulge tester. For example, a P^3 engine has been stacked with the AWGR in series. After the PZT and AWGR were synchronized, i.e., acquired the same frequency and phase, their outputs were added up successfully. This experiment shows the feasibility of cascading many P^3 engines in the future to achieve increased output power.



(a) PCC input voltage

Fig. 6.7. Waveforms for evaluating the efficiency of scheme III with AWGR.



(b) Voltage across R_s

Fig. 6.7. Waveforms for evaluating the efficiency of scheme III with AWGR (continued).

7 CONCLUSIONS

7.1 Conclusions

Advanced low power devices promote the development of micro power generators to replace the batteries to power them. Due to the trend in decreasing the IC supply voltages, power supply designers must face more and more serious challenges. Among these challenges are efficiency, response time, output ripple, size/weight, cost, etc.

A novel power conditioning circuit was proposed to extract maximum power from an MPG. The rectifier stage and the dc-dc regulator stage were designed separately. Three schemes of the rectifier were presented. The proposed rectifier stage is based on the synchronous rectification technique. The dc-dc regulator is a charge pump-based step-down converter to take advantage of the fact that no inductors would be required and that the PZT is capacitive. Interleaved discharge (ID) is proposed to reduce the output voltage ripple greatly, without sacrificing the converter efficiency. The proposed step-down charge pump was analyzed with state-space averaging. Simulation verifies the superiority of the proposed ID method.

In order to facilitate the PZT simulation in PSpice, a simplified PZT model was developed. The parameters in the simplified model can be easily obtained with an HP4284A Precision LCR Meter. This simplified PZT model is very easy to manipulate by PCC designers. The output voltage spectrum of the PZT was analyzed with the Fast Fourier Transform (FFT) so that the PSpice PZT model can generate the same waveforms as the real PZT membranes. After that, three possible rectifier topologies were simulated with PSpice. Because the research on the micro heat engines is still in progress at Washington State University, there exists some uncertainty in the dc link voltage level, i.e., the step-down ratio of the charge pump is unknown. As such, this work designed a generic step-down charge pump. A 5V/1.2V, 200mW, 1% output ripple charge pump was simulated. Simulations show that the

interleaved discharge method takes full advantage of the step-down charge pump structure, and leads to some flexibilities in the design of step-down charge pumps. The designed 5V/1.2V, 200mW charge pump has an efficiency of 92.2%, with reduced output ripple.

Proof-of-concept demonstration includes a 4-stage completely passive charge pump driving an analog wristwatch, proving proper operation of the entire P^3 micro power system. Performance of the proposed PCC is also verified experimentally. A maximum output power of 18.8μW can be extracted from a single piezoelectric MPG, with a rectifier efficiency of 92%.

Arbitrary waveform generator representation (AWGR) of the piezoelectric membrane is also presented. Compared to the bulge tester, the AWGR is programmable, flexible, more robust, and easier to operate. AWGR can be used to evaluate the efficiency of the designed PCC. AWGR facilitates future tests and demonstrates the feasibility of cascading many MPGs to achieve increased output power.

7.2 Suggestions For Future Work

This work has proposed an interleaved discharge-based step-down charge pump to reduce the output voltage ripple. The effectiveness of the ID method was only verified by simulation. Therefore, future work is needed to verify this method experimentally. It is also desirable to integrate the power conditioning circuit on a single chip, with the potential exception of some of the external capacitors that are difficult to integrate on chip with current technology.

BIBLIOGRAPHY

[1] F. Moll, and A. Rubio, "Human Powered Piezoelectric Batteries to Supply Power of Wereables Electronic Devices," *Int. J. Soc. Mater. Eng. Resour.,* Vol. 10, No. 1, Mar. 2002, pp. 34-40.

[2] http://public.itrs.net/Files/2002Update/Home.pdf, "International Technology Roadmap for Semiconductors 2002 Update."

[3] Jan M. Rabaey, Digital Integrated Circuits: a Design Perspective, Prentice Hall, 1995.

[4] N. Mohan, et al, Power Electronics Converters, Applications, and Design, 2nd ed., John Wiley & Sons. INC., New York, 1995.

[5] http://www.darpa.mil/mto/mpg/overview/index.html, "Micro Power Generation: Overview."

[6] N. S. Shenck, and J. A. Paradiso, "Energy Scavenging with Shoe-Mounted Piezoelectrics," *IEEE Micro*, Vol. 21, No. 3, May/June 2001, pp. 30-42.

[7] T. Starner, "Human Powered Wearable Computing," *IBM Syst. J.*, vol. 35, nos. 3/4, 1996, pp. 618-629.

[8] S. Meninger, et al, "Vibration-to-Electric Energy Conversion", *IEEE Trans. VLSI Systems*, vol. 9, 2001, pp. 64-76.

[9] Masakatsu Saka, and Kinya Matsuzawa, "Seiko Human Powered Quartz Watch Overview," *Prospector IX: Human Powered Systems Technologies*, Nov. 2-5, 1997, pp. 359-384.

[10] C. D. Richard., D. F. Bahr, C-G Xu, and R. F. Richards, "MEMS Power: The P^3 System," *Proc. of IECE2001 36th Intersociety Energy Conversion Engineering Conf*., Savannah, GA, 2001.

[11] K. Bruce, "Fabrication and Characterization of a Piezoelectric Membrane Generator," M.S. Thesis, Washington State University, 2001.

[12] E. A. Vittoz, "Micropower Techniques", in *Design of VLSI Circuits for Telecommunication and Signal Processing*, Editors J.E. Franka and Y.P. Tsividis, Prentice Hall, 1994.

[13] S. Whalen, et al., "Design, Fabrication and Testing of the P3 Micro Heat Engine," *Sensors and Actuators*, vol. 104, no. 3, pp. 200-208, 2003.

[14] Bob Richards, private communication.

[15] http://www.elnamagnetics.com/literature/Ferroxcube/power/plandesi.pdf, FERROXCUBE/Philips App. Note: Design of Planar Power Transformers.

[16] Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.

[17] W. S. Harris, and K. D. T. Ngo, "Power Switched-Capacitor DC-DC Converter: Analysis and Design," *IEEE Trans. on Aerospace and Electronic Systems*, vol. 33, No. 2, April 1997, pp. 386-395.

[18] Tanzawa, T., et al, "Circuit Techniques for a 1.8-V-Only NAND Flash Memory," *IEEE J. of Solid-State Circuits, IEEE Journal of*, vol. 37, issue 1, Jan. 2002, pp. 84 –89.

[19] Hairong Yu, and Zhiliang Chen, "A Two-Phase, Four and Five Boosting Ratio, Charge Pump Cell for LCD Driver," *ASIC 2001*, pp. 266 –270.

[20] Monna, G.L.E., et al, "Charge Pump for Optimal Dynamic Range Filters," *ISCAS '94*, vol. 5, pp. 747 –750.

[21] C. K. Tse, S. C. Wong, and M. H. L. Chow, "On Lossless Switched-Capacitor Power Converters," *IEEE. Tran. On Power Electronics*, vol. 10, No. 3, May 1995, pp. 286-291.

[22] F. Moll, and A. Rubio, "An Approach to the Analysis of Wearable Body-Power System," *MIXDES 2000*, June 2000.

[23] W. J. Li, Z. Wen, P. K. Wong, G. M. H. Chan and P. H. W. Leong, "A Micromachined Vibration-Induced Power Generator for Low Power Sensors of Robotic Systems," *Proceedings of the World Automation Congress: 8th International Symposium on Robotics with Applications*, Hawaii, 2000

[24] Rajeevan Amirtharajah, and A. P. Chandrakasan, "Self-Powered Signal Processing Using Vibration-Based Power Generation," *IEEE J. of Solid-State Circuits*, vol. 33, No. 5, May 1998, pp. 687-695.

[25] S. Horowitz, et al, "Technology Development for Self-Powered Sensors," *AIAA Paper 2002-2702*, *the 1st Flow Control Conference*, June 2002.

[26] G. K. Ottman, et al, "Adaptive Piezoelectric Energy Harvesting Circuit for Wireless Remote Power Supply," *IEEE Trans. on Power Electronics*, vol. 17, No. 5, Sep. 2002, pp. 669-676.

[27] B. Jaffe, W. R. Cook, and H. Jaffe, Piezoelectric Ceramics, Academic Press, London, 1971.

[28] J. D. Hall, N. E. Apperson, B. T. Crozier, C. Xu, R. F.Richards, D. F. Bahr, and C. D. Richards, "A Facility for Characterizing the Dynamic Mechanical Behavior of Thin Film Membranes for Microelectromechanical Systems", *Review of Scientific Instruments*, vol. 73, pp. 2067-2072, 2002.

[29] R. Krishnan, Electric Motor Drives: Modeling, Analysis & Control, Prentice Hall, Upper Saddle River, N. J., 2001.

[30] http://www.formfactors.org/developer/specs/atx/atx12vPSDGV1.pdf, "ATX/ATX12V Power Supply Design Guide."

[31] Chin Chang, and Mike A. Knights, "Interleaving Technique in Distributed Power Conversion Systems," *IEEE Trans. Circuit and Systems*, vol. 42, No., 5, May 1995, pp. 245-251.

[32] R. Giral, et al, "Interleaved Converters Operation Based on CMC," *IEEE Trans. Power Electronics*, vol. 14, No. 4, July 1999, pp. 643-651.

[33] Peng Xu, et al, "A Family of Novel Interleaved DC/DC Converters for Low-Voltage High-Current Voltage Regulator Module Applications," *Power Electronics Specialists Conference*, vol. 3, June 2001, pp. 1507 –1511.

[34] D. J. Perreault, and J. G. Kassakian, "Distributed Interleaving of Paralleled Power Converters," *IEEE Trans. Circuit and Systems*, vol. 44, No., 8, Aug. 1997, pp. 728-734.

[35] Seung-Chul Lee, et al, "A Low-Ripple Switched-Capacitor DC-DC up Converter for Low-Voltage Applications," *ASICs, Proceedings of the Second IEEE Asia Pacific Conference on*, 28-30 Aug., 2000, pp. 13 –16.

[36] National Semiconductor Corporation, "LM2781 Ultra-Low Ripple Switched Capacitor Voltage Inverter."

[37] P. M. Lin and Leon O. Chua, "Topological Generation and Analysis of Voltage Multiplier Circuits," *IEEE Trans. on Circuits and Systems*, vol. CAS-24, No. 10, Oct. 1977, pp. 517-530.

[38] A. S. Sedra, and K. C. Smith, Microelectronics Circuits, 4th ed., Oxford University Press, New York, 1998.

[39] http://pdfserv.maxim-ic.com/arpdf/ICL7660-MAX1044.pdf.

[40] S. V. Cheong, et al, "Inductorless DC-to-DC Converter with High Power Density," *IEEE Trans. on Industrial Electronics*, vol. 41, No. 2, April 1994, pp. 208-215.

[41] Henry Chung, et al, "Design and Analysis of Multi-Stage Switched-Capacitor-Based Step-Down DC/DC Converters," *PESC 98 Record*, 29th Annual IEEE, vol. 2, May 1998, pp. 1655 –1661.

[42] Henry S. H. Chung, "Development of DC/DC Regulators Based on Switched-Capacitor Circuits," *Proceedings of the 1999 IEEE International Symposium on*, vol. 5, 30 May-2 June 1999, pp. 210 –213.

[43] R.D. Middlebrook, and S. Ćuk, "A General Unified Approach to Modeling Switching-Converter Power Stages," *IEEE Power Electronics Specialists Conference Record*, June 1976, pp. 18-34.

[44] S. Sherrit, H. D. Wiederick, and B. K. Mukherjee, "Accurate Equivalent Circuits for Unloaded Piezoelectric Resonators," *IEEE Ultrasonics Symposium 1997*, pp. 931-935.

[45] Curtis D. Johnson, Handbook of Electrical and Electronics Technology, Englewood Cliffs, N.J.: Prentice Hall, 1996.

[46] http://pdfserv.maxim-ic.com/en/ds/MAX9117-MAX9120.pdf, "SC70, 1.8V, Nanopower, Beyond-the-Rails Comparators With/Without Reference."

APPENDICES

APPENDIX A. PSpice Simulation Netlists

1. Netlist for Fig. 2.18

```
* source NGO_1997
D_D2B         0 N80886 D1N5822 5
D_D3B         0 N17346 D1N5822 5
D_D4B         0 N17337 D1N5822 5
V_Vgs1        N78003 N78239
+PULSE 0 5.205 0us 0.1us 0.1us 2.5us 10us
M_S4          N78239 N82338 N17449 N17449 IRF520
V_Vqs2        N82338 N17449
+PULSE 0 10 2.7us 0.1us 0.1us 7us 10us
M_S2          N17475 N82338 N17449 N17449 IRF520
M_S3          N17510 N82338 N17449 N17449 IRF520
C_C4          N17334 N78239  9.6uF
C_C3          N17343 N17510  9.6uF
C_C1          0 N17449  86.4uF
C_C2          N173000 N17475  9.6uF
R_RL          0 N17449  3
R_Rc3         N17346 N17343  0.003
R_Rc4         N17337 N17334  0.003
R_Rc2         N80886 N173000  0.003
V_Vs          N84845 0 55V
M_Sc          N84845 N78003 N78239 N78239 IRF520
D_D4A         N17337 N17510 D1N5822 5
D_D2A         N80886 N17449 D1N5822 5
D_D3A         N17346 N17475 D1N5822 5
```

2. Netlist for Fig. 2.20

```
* source NGO_1997_MY
D_D4B         0 N17337 D1N5822 5
D_D3B         0 N17346 D1N5822 5
D_D2B         0 N80886 D1N5822 5
V_Vqs1        N78003 N78239
+PULSE 0 5.8 0us 0.1us .1us 2.5us 10us
V_Vqs2        N82516 N17449
+PULSE 0 10 2.6us 0.1us .1us 2.26us 10us
M_S4          N78239 N87660 N17449 N17449 IRF520
M_S3          N17510 N82531 N17449 N17449 IRF520
M_S2          N17475 N82516 N17449 N17449 IRF520
V_Vqs4        N87660 N17449
+PULSE 0 10 7.52us 0.1us .1us 2.26us 10us
V_Vqs3        N82531 N17449
+PULSE 0 10 5.06us 0.1us .1us 2.26us 10us
C_C4          N17334 N78239  9.6uF
C_C2          N17352 N17475  9.6uF
C_C1          0 N17449  86.4uF
C_C3          N17343 N17510  9.6uF
R_Rc3         N17346 N17343  0.003
R_RL          0 N17449  3
R_Rc2         N80886 N17352  0.003
R_Rc4         N17337 N17334  0.003
V_Vs          N17562 0 55V
M_Sc          N17562 N78003 N78239 N78239 IRF520
D_D4A         N17337 N17510 D1N5822 5
D_D3A         N17346 N17475 D1N5822 5
D_D2A         N80886 N17449 D1N5822 5
```

3. Netlist for Fig. 3.7

```
* source rectifier_scheme_1
V_V2         N000660 N000661
+SIN 0 0.5822 800 0 0 90
V_V3         N000661 N000701
+SIN 0 0.0417 1200 0 0 90
V_V4         N000701 N000741
+SIN 0 0.0143 1600 0 0 90
V_V5         N000741 N000781
+SIN 0 0.017 2000 0 0 90
C_Co         0 N01610  10u
V_V6         N000781 N009411
+SIN 0 0.0111 2400 0 0 90
V_V1         N00018 N000660
+SIN 0 1 400 0 0 90
R_Rs         N08732 N10147  470
C_Cs         N00018 N08732  31.4n
R_Rc         0 N10147  40k
D_D1         N10147 N01610 D1N4152
V_V7         N009411 0
+SIN 0 0.0122 2800 0 0 90
R_RL         0 N01610  80k
```

4. Netlist for Fig. 3.11

```
* source rectifier_scheme_2
V_V5         N000741 N000781
+SIN 0 0.017 2000 0 0 90
V_V4         N000701 N000741
+SIN 0 0.0143 1600 0 0 90
V_V3         N000661 N000701
+SIN 0 0.0417 1200 0 0 90
V_V2         N000660 N000661
+SIN 0 0.5822 800 0 0 90
C_Co         0 N01610  10u
V_V1         N00018 N000660
+SIN 0 1 400 0 0 90
V_V6         N000781 N009411
+SIN 0 0.0111 2400 0 0 90
C_Cs         N00018 N08732  31.4n
R_Rs         N08732 N10147  470
D_D2         0 N10147 D1N4152
D_D1         N10147 N01610 D1N4152
V_V7         N009411 0
+SIN 0 0.0122 2800 0 0 90
R_RL         0 N01610  80k
```

5. Netlist for Fig. 3.13

```
* source rectifier_scheme_3
.EXTERNAL INPUT 3
.EXTERNAL INPUT -3
V_V5        N000741 N06359
+SIN 0 0.017 2000 0 0 90
V_V4        N000701 N000741
+SIN 0 0.0143 1600 0 0 90
V_V3        N00087 N000701
+SIN 0 0.0417 1200 0 0 90
V_V2        N00957 N00087
+SIN 0 0.5822 800 0 0 90
X_Q1        N18570 N07657 N06176 BS170/SIE
X_Q2        N17462 0 N07657 BS170/SIE
V_V6        N06359 N07280
+SIN 0 0.0111 2400 0 0 90
V_V1        N01063 N00957
+SIN 0 1 400 0 0 90
R_Rs        N08224 N07657  470
C_Cs        N01063 N08224  31.4n
C_C0        0 N06176  10u
D_D2        0 N07657 D1N4152
D_D1        N07657 N06176 D1N4152
R_RL        0 N06176  80k
X_U1A       N07657 N06176 3 -3 N18728 MAX922/MXM
V_V9        3 0 3V
V_V8        -3 0 -3V
C_C3        0 N18570  .1uF
R_R8        N18570 N18728  10
V_V7        N07280 0
+SIN 0 0.0122 2800 0 0 90
X_U2A       0 N07657 3 -3 N17462 MAX922/MXM
```

6. Netlist for Fig. 3.16

```
* source CP_conventional
M_S4B         N17337 N86153 0 0 IRFZ34
V_Vqsa        N78003 0
+PULSE 0 10 0us 0.1us .1us 2.5us 10us
V_Vqs1        N86153 N17452
+PULSE 0 10 2.7us 0.1us .1us 7us 10us
C_C4          N17334 N82294  10uF
C_C3          N17343 N17512  10uF
C_C1          0 N17452  50uF
C_C2          N90443 N87431  10uF
M_S2B         N84728 N86153 0 0 IRFZ34
M_S3B         N17346 N86153 0 0 IRFZ34
R_RL          0 N17452  7.2
R_Rc3         N17346 N17343  0.003
R_Rc4         N17337 N17334  0.003
R_Rc2         N84728 N90443  0.003
V_Vs          N17559 0 5V
M_S4          N82294 N86153 N17452 N17452 IRFZ34
M_S3          N17512 N86153 N17452 N17452 IRFZ34
M_S2          N87431 N86153 N17452 N17452 IRFZ34
M_S4A         N17512 N87759 N17337 N17337 IRFZ34
V_Vqsb        N87759 0
+PULSE 0 10 0us 0.1us .1us 2.5us 10us
M_S3A         N87431 N87759 N17346 N17346 IRFZ34
M_Sc          N17559 N78003 N82294 N82294 IRF520
M_S2A         N17452 N87759 N84728 N84728 IRFZ34
```

7. Netlist for Fig. 3.18

```
* source CP_ID
V_Vqs4         N88378 0
+PULSE 0 10 7.5us 0.1us .1us 2.2us 10us
V_Vqs3         N81488 0
+PULSE 0 10 5.1us 0.1us .1us 2.2us 10us
M_S4B          N17337 N88378 0 0 IRFZ34
V_Vqsa         N78003 0
+PULSE 0 10 0us 0.1us .1us 2.5us 10us
V_Vqs2         N86861 0
+PULSE 0 10 2.7us 0.1us .1us 2.2us 10us
C_C4          N17334 N82294  10uF
C_C3          N17343 N17512  10uF
C_C1          0 N17452  22uF
C_C2          N173000 N17477  10uF
M_S2B          N84728 N86861 0 0 IRFZ34
M_S3B          N17346 N81488 0 0 IRFZ34
R_RL          0 N17452  7.2
R_Rc3          N17346 N17343  0.003
R_RC4          N17337 N17334  0.003
R_Rc2          N84728 N173000  0.003
V_Vs          N17562 0 5V
M_S4          N82294 N88378 N17452 N17452 IRFZ34
M_S2          N17477 N86861 N17452 N17452 IRFZ34
M_S3          N17512 N81488 N17452 N17452 IRFZ34
M_S4A          N17512 N84387 N17337 N17337 IRFZ34
V_Vqsb         N84387 0
+PULSE 0 10 0us 0.1us .1us 2.5us 10us
M_S3A          N17477 N84387 N17346 N17346 IRFZ34
M_M25          N17562 N78003 N82294 N82294 IRF520
M_S2A          N17452 N84387 N84728 N84728 IRFZ34
```

APPENDIX B. Operation Instructions for the Proof-of-Concept Demonstration Circuit

The operating positions of the toggle switches are labeled in Fig. 4-2. TS1~TS3 all have three positions. TS4 has two positions.

1) To charge the capacitors, pull the handles of TS1~TS4 to position 1 (see Fig. 4.2). Measure the voltage $V_{parallel}$ between the cathode of diode D1 and OUT-. It can be found that the voltage slowly increases. When $V_{parallel}$ = 0.39V, pull all switches to position 2 following the order of TS4, TS3, TS2, and TS1. (MUST! Otherwise the capacitors may get discharged!)

2) By pulling TS1 to position 3, and TS2 to position 3, the four capacitors will be re-connected in series. Measure the voltage V_o between OUT+ and OUT- (test points P+ and P- can be used for convenience), it should be V_o= $V_{parallel}$*4=0.39V*4=1.56V. Note, it will be observed that V_o keeps decreasing, even though the watch is not connected. This is due to the leakage current of the capacitors.

Make sure V_o is less than 1.58V, and then connect the watch to OUT+ and OUT-. Please make sure the polarities are correct. Note, the negative input of the watch can be connected to OUT- all the time, this will save the wire-connecting time. A rapid connecting operation can lead to a longer running time of the watch.

APPENDIX C. Operation Instructions for the AWGR

The output waveform of a PZT membrane has already been imported into the 'USR2' function of AFG310. A picture of AFG310 is shown below.

1) Turn on the power of AFG310
2) Press the 'FUNC' button on the upper right of the front panel, scroll up or down by pressing INC/DEC control buttons, when 'USR2' function appears, select it by pressing the 'ENTER' button
3) Press the 'FREQ' button on the upper right of the front panel, key in 100 (Hz) for the frequency from the numeric input keys, and press the 'ENTER' button
4) Press the 'AMPL' button on the upper right of the front panel, key in 2.92 (V) for the amplitude from the numeric input keys, and press the 'ENTER' button
5) Press the output button, and the output indicator should turn on
6) Observe the output waveform with an oscilloscope, the shape of the waveform should look like that of a PZT membrane, the frequency should be 400Hz, and the peak-to-peak amplitude should be 2.5V

APPENDIX D. Publications

Universal Power Supply Approach for Improved Ride-Through in Industrial Drives

Jifeng Han, Annette von Jouanne, and Alan K. Wallace
Power Electronics Laboratory
Department of Electrical and Computer Engineering
Oregon State University
Corvallis, OR 97331-3211
Tel: (541) 737-0831
Fax: (541) 737-1300
Email: han@ece.orst.edu; avj@ece.orst.edu; wallace@ece.orst.edu

***Abstract* - This paper summarizes current designs of power supplies (PS's) for industrial drives and presents a novel universal switch-mode power supply (SMPS) approach. Adjustments to the switching algorithm and transformer turns ratio are presented to improve ride-through characteristics and allow the SMPS to operate as a universal supply over a wide input voltage range, without the additional circuitry of current universal PS systems. The proposed approach can also overcome potential safety issues of common universal PS's and is equally suitable to meet the requirements of many commercial systems. Simulation and experimental results on a 100W (5V/20A) half-bridge SMPS are provided to demonstrate the proposed approach.**

I. INTRODUCTION

Power supplies are of importance to many commercial and industrial electrical systems and can be vulnerable to power system voltage sags and momentary interruptions. Example sensitive equipment includes computers, communication equipment, adjustable speed drives (ASDs) and a variety of aerospace/military devices. When this type of equipment suffers momentary interruptions or permanent trips, the result can be significant downtime and losses [1]-[6].

In recent years, ASD ride-through has gained increased attention [6]-[12]. In the case of ASDs, two major reasons for tripping have been identified [5], [6]:

a) Insufficient voltage for maintaining the ASD's internal power supply voltages for the logic and control circuits. For a 460V ASD whose internal power supply is derived from the ac-line, the "control power low" trip settings for single-phase, two-phase and three-phase voltage sags are typically around 65%, 30% and 20%, respectively, of the nominal ac voltage [13].

b) Insufficient voltage for maintaining the operation of the motor at the desired speed/torque set point. The under-voltage trip point varies from manufacturer to manufacturer and depends on the application. Typical under-voltage dc-bus trip settings for a 460V ASD range from about 480V - 585V, or from 75-90% of the nominal dc-bus voltage.

Both of the above reasons for ASD tripping occur due to a reduction, or interruption, of the ac input voltages to the drive. A common assumption is that reductions and interruptions in the ac voltages supplying drives are a direct result of an event on the utility electric power system causing the drive to trip. However, the problem often lies in the external circuits that interface directly with a drive to control functions and operations such as "start/stop" and "enable" [5]. Most often these devices are powered by single-phase sources, making them susceptible to single-phase events, and potentially more prone to tripping than the drive.

Much attention has been paid recently to ASD ride-through programming features [6], addressing external interface and control circuits, and providing a means for maintaining dc-bus voltages. Little work has been done on making the internal power supply more robust to disturbances.

Thus, this paper endeavors to develop a universal power supply approach (UPSA) that will provide additional ride-through for both commercial and industrial switch-mode power supply (SMPS) systems. For this universal approach, the power supply input voltage can vary within a given range, while the output remains within the specified tolerances.

In section II, presently available universal power supply systems are reviewed. Section III proposes an automatic, efficient, cost effective and reliable UPSA that can be driven by a wide input range, for both commercial and industrial systems. Section IV presents simulation and experimental results on a on a 100W (5V/20A) half-bridge SMPS. Finally, section V draws conclusions.

II. PRESENTLY AVAILABLE UNIVERSAL POWER SUPPLY SYSTEMS

Most modern universal power supplies utilize a standard approach to provide the required output voltage. The power supply circuitry typically comprises a rectifier, a dc/dc converter with isolation transformer, and a manual switch to select input range. As shown in Fig. 1, a manual switch is included in the voltage-doubler rectifier to accommodate 115 Vac or 230 Vac input. When the switch is in the 230V position with a line voltage of 230V, the circuit acts as a bridge

rectifier. With the switch in the 115V position and the line voltage of 115V, the circuit acts as a voltage doubler. This design has a potential safety issue, i.e., if a unit set for 115 Vac is connected to 230 Vac, damage may occur.

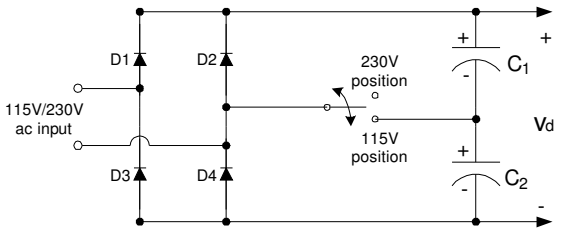


Fig. 1 A voltage-doubler rectifier used in common universal power supplies.

It is also common practice to provide a dc/dc converter, such as a pulse-width modulated chopper to convert a single-phase ac power supply into a dc voltage for electric arc welding or plasma cutting [14]. These power supplies are specifically designed for 60Hz, 110V or 220V input. The circuitry is made up of a dual stage power supply including a first stage inverter with an active, switching type power factor correcting circuit to provide controlled dc input to the second stage inverter. This use of a two-inverter two-stage power supply for providing the power factor corrections and at the same time controlling the dc voltage at the output is complicated and expensive.

Survey [15] shows that typical ac/dc switching power supplies have universal input voltages, i.e., both 115 Vac and 230 Vac, and example power ratings are as follows:

- Personal computers 100-400 W
- Workstations 100-750 W
- Telecommunications 50-500 W
- Medical instruments < 100 W
- Process control equipment 100-700 W

To determine the types of power supply configurations used in industrial applications such as ASDs, the authors conducted a survey with the results shown in Table I. Note, when the internal power supply input voltage is derived off the dc-bus, the ASD is less susceptible to ride-through disturbances.

TABLE I CONFIGURATIONS OF ASD INTERNAL POWER SUPPLIES

ASD Manufacturers	Type of internal power supply		
	Switch- Mode derived from ac input	dc-Bus Converter	Linear
A	X		
B		X	
C		X	
D	X		
E		X	
F		X	
G	X		X
H		X	

III. PROPOSED UPSA

To realize the proposed UPSA, modifications are made to a common SMPS. The transformer output voltage is increased by reducing the turns ratio, thus allowing the duty cycle to be reduced for nominal input and output voltages. Hence, as the input voltage decreases, the duty ratio is automatically increased to maintain an acceptable power supply output voltage, i.e., to provide the power supply with enhanced ride-through, without the additional circuitry required in current systems as described in section II. For a standard half-bridge converter, the duty cycle has a maximum of 0.5. Considering dead time, the duty cycle of an SMPS is usually between 0.2 and 0.47 [16].

IV. SIMULATION AND EXPERIMENTAL RESULTS

Fig.2 shows the PSpice simulation schematic demonstrating the proposed UPSA that can be used in single-phase commercial applications. A standard half-bridge converter topology is adopted, which is the most popular topology in a typical computer-based SMPS [17], [18], except in the proposed approach, the transformer turns ratio is modified. The SMPS is a 100W, 120V input and 5V output unit. For computer-based systems, the output tolerance is ±5% (±0.25V for a 5V nominal output) as dictated in [19], [20]. The simulation results are given in Fig. 3. In Fig. 3 (a), for the original (typical) transformer with turns ratio n=12:1, when $V_{in,rms}$=120V, to maintain the nominal output voltage, the duty cycle is D=0.23. However, as shown in Fig. 3 (b), after a 29% sag (71% remaining voltage), D will have to exceed 0.47, which is prohibited for a half-bridge converter because of the dead time needed. For the proposed approach, the transformer turns ratio is reduced to n=8:1. Thus, as shown in Fig. 3 (c) and (d), when the input voltage $V_{in,rms}$=120V, the duty cycle D=0.13; when $V_{in,rms}$=60V, due to a 50% voltage sag, the duty cycle is increased automatically, and D_{max}=0.47. Thus, the power supply can maintain nominal output voltages and ride through a 50% voltage sag.

The proposed approach was then applied to a 100W (5V/20A) personal computer power supply. The experimental results are shown in Fig.4. In Fig. 4 (a), for the original (typical) transformer with turns ratio n=12:1, when $V_{in,rms}$=120V, to maintain the nominal output voltage, the duty cycle is D=0.21. However, as shown in Fig. 4 (b), after a 35% sag (65% remaining voltage), the output voltage will fall out of the required tolerance. For the proposed approach, the transformer turns ratio is decreased to n=8:1. Thus, as shown in Fig. 4 (c) and (d), when the input voltage $V_{in,rms}$=120V, the duty cycle D=0.14; when $V_{in,rms}$=60V, due to a 50% voltage sag, the duty cycle is increased automatically, and D=0.4. Thus, the power supply can maintain nominal output voltages and ride through a 50% voltage sag.

The simulation and experimental results show that the proposed approach can provide 50% ride-through for single-

phase computer-based power supply systems. If applied to 230V-input power supplies, it can still operate within tolerances when the input voltage drops to 115V. The manual switch in a common power supply can thus be cancelled, and the potential safety issue of applying the 115V setting to 230V no longer exists.

V. CONCLUSIONS

This paper presents a new universal power supply approach (UPSA) to automatically provide nominal output voltages under a wide range of input voltage conditions, without the additional circuitry of current universal power supply systems. Thus UPSA-based PS's can overcome the potential safety issue of a common universal power supply. Simulation and experimental results show that the proposed approach can provide 50% ride-through for single-phase computer-based power supply systems through simple modifications to the transformer turns ratio and switching duty cycle. This approach can be applied to both commercial and industrial systems.

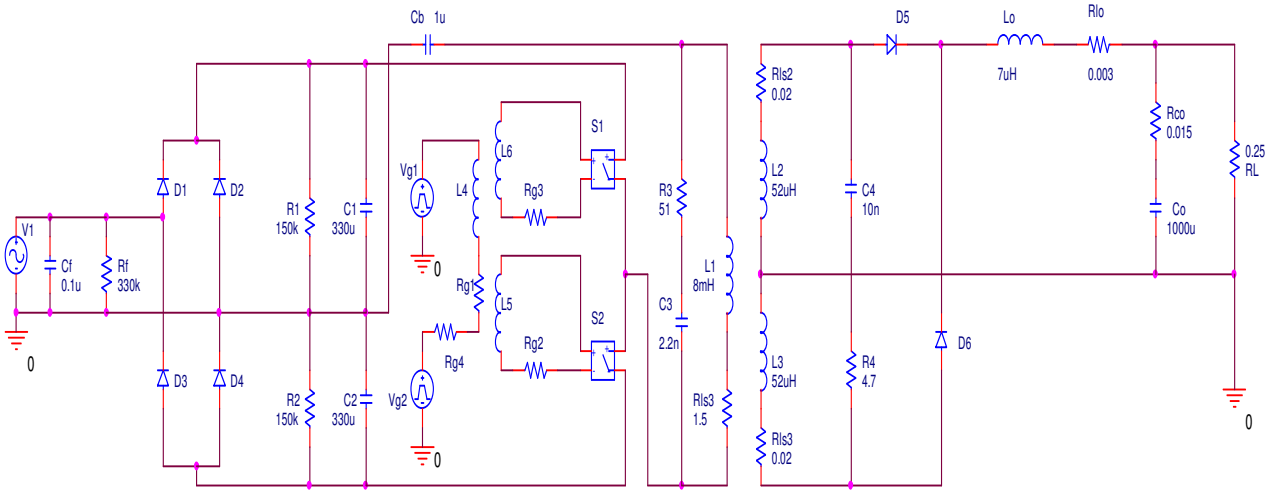


Fig.2 Simulation schematic for the proposed UPSA.

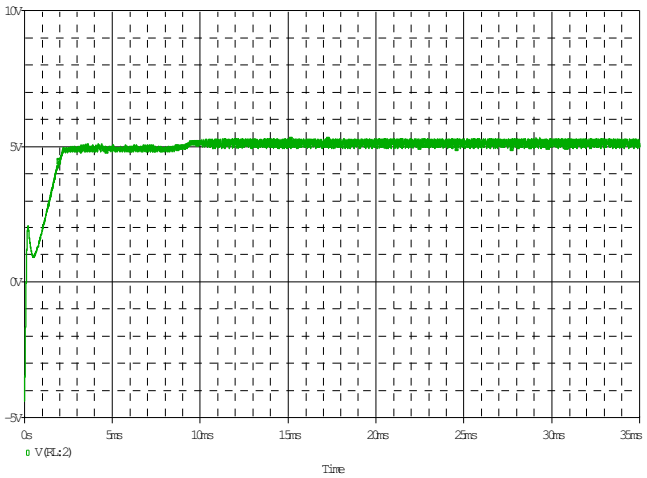


Fig.3 (a) Typical transformer turns ratio n=12:1, $V_{in,rms}$=120V, D=0.23, Vo=5.05.

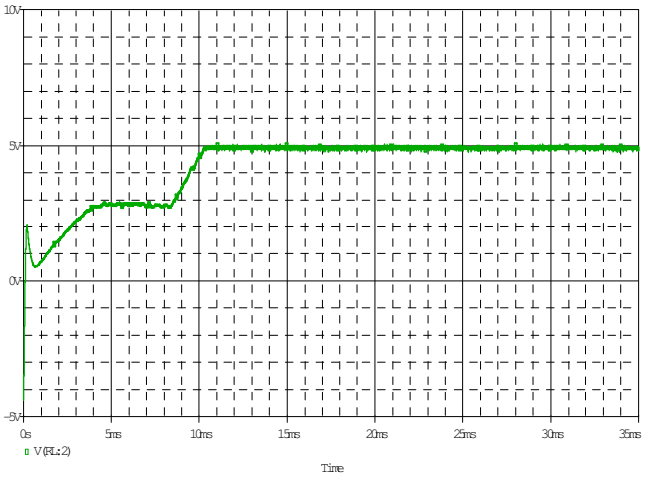
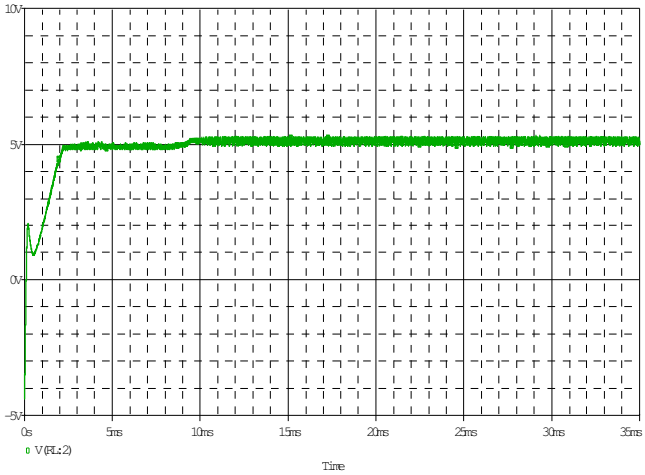
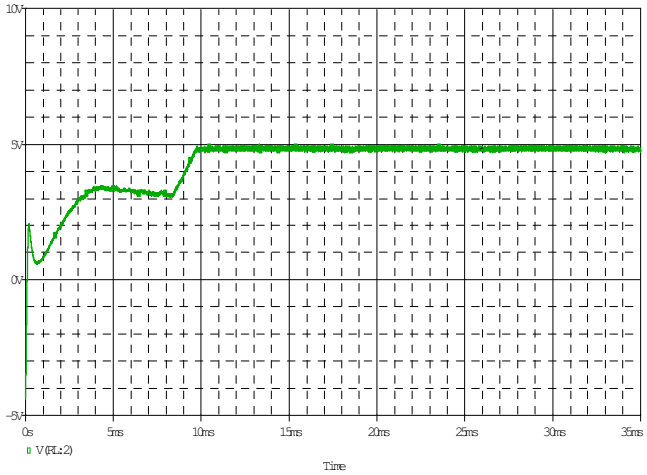


Fig.3 (b) Typical transformer turns ratio n=12:1, $V_{in,rms}$=84.85V (29% voltage sag), D_{max}=0.47, Vo=4.89V.

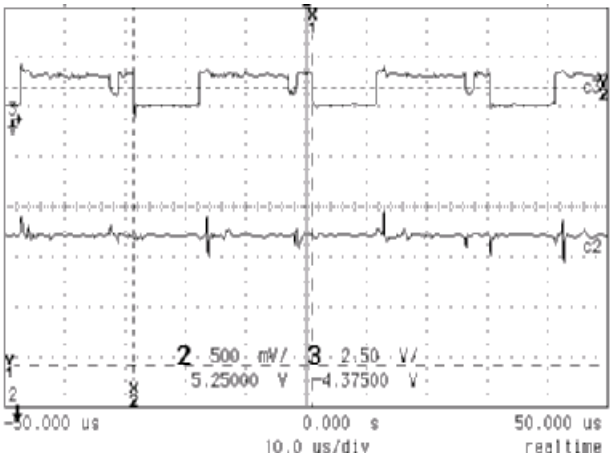


(c) Proposed transformer turns ratio n=8:1, $V_{in,rms}$=120V, D=0.13, Vo=5.11V.

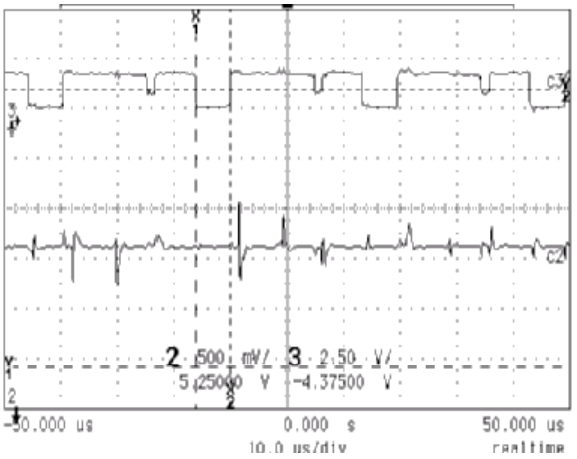


(d) Proposed transformer turns ratio n=8:1, $V_{in,rms}$=60V (50% voltage sag), D_{max}=0.47, Vo=4.82V.

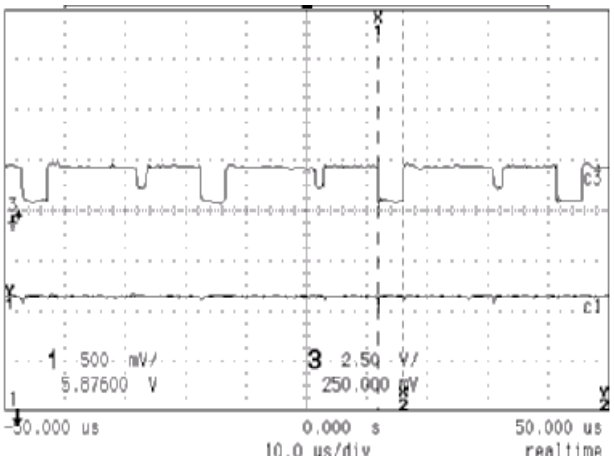
Fig.3 Simulation results for a typical PS, and the proposed UPSA.



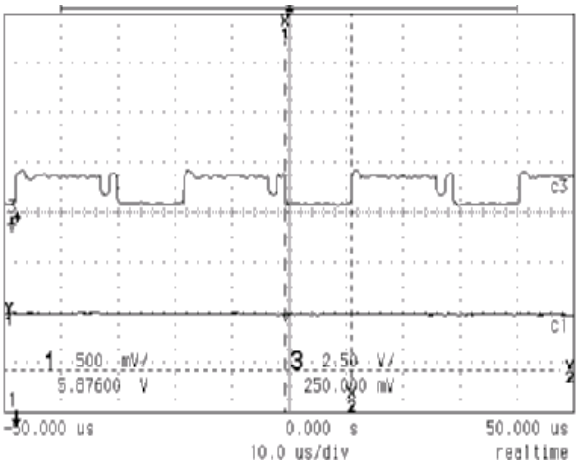
(a) Typical PS, $V_{in,rms}$ =120V, D=0.21, Vo=5V.



(b) Typical PS, $V_{in,rms}$ =78V (35% voltage sag), D=0.36, $V_{o,min}$=4.8V.



(c) Proposed, $V_{in,rms}$ =120V, D=0.14, Vo=5V.



(d) Proposed, $V_{in,rms}$ =60V (50% voltage sag), D=0.4, $V_{o,min}$=4.75V.

Fig.4 Experimental Results for a typical PS, and the proposed UPSA

REFERENCES

[1] Information Technology Industry Council (ITI), "ITI (CBEMA) Curve Application Note", http://www.itic.org/technical/iticurve.pdf.

[2] F. Carlsson, B. Widell, C. Sadarangani, "Ride-Through Investigations for a Hot Rolling Mill Process", Power System Technology, 2000. Proceedings, PowerCon 2000, International Conference on, vol.3, Dec. 2000, pp.1605 – 1608.

[3] V. J. Gosbell, V. Smith, D. A. Robinson, B.S.P. Perera, R. Coulter, "Sag Testing of Dairy Farm Milking Equipment", Power System Technology, 2000, Proceedings, PowerCon 2000, International Conference on, vol.2, Dec. 2000, pp.947-952.

[4] A. von Jouanne, P. N. Enjeti, B. Banerjee, "Assessment of Ride-Through Alternatives for Adjustable-Speed Drives", Industry Applications, IEEE Transactions on , vol.35, July-Aug. 1999, pp.908 – 916.

[5] R. Langley, A. Mansoor, " What Causes ASDs to Trip During Voltage Sags? – Parts 1-4", Power Quality Assurance Magzine, Sept. – Dec. 1999.

[6] A. von Jouanne, B. Ben Banerjee, "Ride-through Alternatives for AC and DC Drives Including Medium Voltage (2300/4160V) Multi-level Inverters", PQA 2000 Conference Proceedings.

[7] A. van Zyl, R. Spee, A. Faveluke, S. Bhowmik, "Voltage Sag Ride-Through for Adjustable-Speed Drives with Active Rectifiers", Industry Applications, IEEE Transactions on, vol. 34, Nov.-Dec. 1998, pp.1270-1277.

[8] N. S. Tunaboylu, E. R. Collins, Jr., S. W. Middlekauff, R. L. Morgan, "Ride-Through Issues for DC Motor Drives During Voltage Sags", Southeastcon '95. Visualize the Future., Proceedings., IEEE, March 1995,pp.52–58.

[9] J. L. Duran-Gomez, P.N. Enjeti, Byeong Ok Woo, "A Low Cost Approach to Improve the Performance of an Adjustable Speed Drive (ASD) under Voltage Sags and Short-Term Power Interruptions", Power Electronics congress, 1998. CIEP 98. VI IEEE International, Oct. 1998, pp. 16 – 21.

[10] J. L. Duran-Gomez, P.N. Enjeti, Byeong Ok Woo, "Effect of Voltage Sags on Adjustable-Speed Drives: a Critical Evaluation and an Approach to Improve Performance", Industry Applications, IEEE Transactions on, vol. 35, Nov.-Dec. 1999, pp.1440 – 1449.

[11] M. Corley, J. Locker, S. Dutton, R. Spee, "Ultracapacitor-Based Ride-Through System for Adjustable Speed Drives", Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE, vol.1, 27 June-1 July 1999, pp. 26 – 31.

[12] Yong-Seok Kim, Seung-Ki Sul, "A Novel Ride-Through System for Adjustable Speed Drives Using Common-Mode Voltage", Industry Applications Conference, 2000. Conference Record of the 2000 IEEE, vol.4, Oct. 2000, pp.2440 – 2447.

[13] Evelyn Matheson, "A remotely Controlled Power Quality Test Platform for Characterizing the Ride-Through Capabilities of Adjustable Speed Drives", M.S. thesis, Oregon State University, 2001.

[14] T.E.Kooken, U. S. Pat. No. 5,991,169, Lincoln Global, Inc., Nov.23, 1999.

[15] M. Klapfish, "Trends in AC/DC Switching Power Supplies and DC/DC Converters", Applied Power Electronics Conference and Exposition, 1993. APEC '93. Conference Proceedings 1993, Eighth Annual, pp. 87 –91.

[16] Texas Instruments, "Designing Switching Voltage Regulators with TL494", http://www-s.ti.com/sc/psheets/slva001a/slva001a.pdf.

[17] R.E. Tarter, Solid-State Power Conversion Handbook, John Wiley & Sons, INC., New York, 1993.

[18] Intel Company, "PC Design Considerations: Power Supply Unit", http://developer.intel.com/design/quality/pcdesign/psu.htm.

[19] Astec's 145W Platform, http://www.astec.com/products/datasheets.-htm1#pc, pp2.

[20] Unitrode Application Notes, http://www-s.ti.com/sc/psheets/slus223 /slus223.pdf, pp7.

Novel Power Conditioning Circuits for Piezoelectric Micro Power Generators

Jifeng Han, Annette von Jouanne, Triet Le, K. Mayaram, T. S. Fiez
School of Electrical Engineering and Computer Science
Oregon State University
Corvallis, OR 97331-3211
Tel: 541-737-0831, Fax: 541-737-1300
avj@ece.orst.edu

Abstract – **Low power devices promote the development of micro power generators (MPGs). This paper presents a novel power conditioning circuit (PCC) that enables maximum power extraction from a piezoelectric MPG. Synchronous rectification (SR) is employed to improve the PCC efficiency. A simplified model of the piezoelectric generator is developed for simulation. Performance of the proposed PCC is verified by PSpice simulation and experimental results. A maximum output power of 18.8μW has been extracted from a single piezoelectric MPG, with 92% efficiency of the PCC. Arbitrary waveform generator representation (AWGR) of the piezoelectric membrane is also presented. AWGR facilitates future tests and demonstrates the feasibility of cascading many MPGs to extract additional power. Future work will include integrating the PCC on a single chip.**

I. INTRODUCTION

The appearance of wearable electronic devices, such as mobile telephones and "Personal Digital Assistants" (PDAs) among others, has transformed the way people communicate and network. Wireless integrated network sensors (WINS) are widely used in civil and military applications. Advances in integrated circuit technology, following Moore's Law, have enabled the reduction of the size/weight and energy requirement of these devices. For example, by 2005, the power consumption of the Bluetooth communication technique will drop to 5.1mW [1]. Usually, the above low power devices are powered by bulky batteries with a short service life. Battery replacement may also be difficult in applications such as unattended sensors.

An attractive alternative to batteries is micro power generators (MPGs), which have recently gained increased attention. An MPG is expected to be five-to-ten times smaller than a comparable battery [2], and features enhanced performance. Some MPGs can scavenge attainable energy from the environment of the system and convert it into useful electrical energy [3]-[5]. Feasibility of scavenging energy from human body/activities has been studied [1], [3], [6]. In [6], it is estimated that at least 500mW of useful electrical power can be harvested from usual clothes such as a cap. Therefore, it is possible to feed wearable systems from body heat dissipation via electrothermal conversion. In [3], researchers demonstrated that when people walk, parasitic power in shoes could be harvested to power a radio frequency tag that transmits a short-range, 12-bit wireless identification (ID) code. Other attainable ambient energy sources include mechanical energy [5], acoustic energy [7], etc. In [5], a system was proposed to convert ambient mechanical vibration into electrical energy, with an approximate net output power of 8μW.

However, little attention has been paid on how to extract maximum power from MPGs. In [8], an adaptive piezoelectric energy harvesting circuit was proposed to harvest maximum power from the vibrating piezoelectric transducer. However, the first stage of this circuit is a simple diode bridge rectifier, which is unsuitable for low-voltage MPGs whose output voltage is comparable to a diode forward voltage drop.

This paper will focus on the design of a power conditioning circuit (PCC) for use in conjunction with the MEMS-based P^3 micro heat engine power generation system proposed by researchers at Washington State University [9]. A single P^3 micro heat engine is expected to provide 1mW of continuous power with a power density of ~1W/cm^3 and energy density of ~1000Whr/kg. This paper proposes a novel PCC based on synchronous rectification and charge pump techniques. The PCC draws useful electric power from the P^3 engine and converts it to the regulated voltage. In low-output-voltage switch-mode power supplies (SMPSs), synchronous rectification (SR) has already been widely applied to improve power supply efficiency [10]. In this paper, SR is applied to the PCC for improved efficiency. The proof-of-concept demonstration includes a manually operated charge pump and a 1.5V analog watch.

This paper is organized as follows. Section II presents proof-of-concept demonstration and proposes the novel PCC. In section III, the proposed PCC is verified by PSpice simulation. The experimental setup, results and discussion are presented in sections IV and V, respectively. Arbitrary waveform generator representation (AWGR) of the PZT membrane is presented in section VI. Finally, section VII summarizes this paper and discusses future work.

II. POWER CONDITIONING CIRCUIT

In the P^3 engine, piezoelectric membranes generate an unregulated ac voltage. However, the targeted loads require regulated dc voltage. Therefore, a PCC is needed to draw useful electric power from the P^3 engine and convert it to the regulated dc voltage. The PCC should also provide impedance matching between the P^3 engine and the load, for maximum power delivery. The proposed PCC includes two stages: a rectifier as the first stage, and a dc-dc converter as the second stage. In an effort to achieve miniaturization, it is desirable to integrate the PCC on a single chip. Conventional dc-dc converters such as buck-boost converters feature high efficiency but they need bulky magnetic components. The charge pump is a promising dc-dc converter in that it is

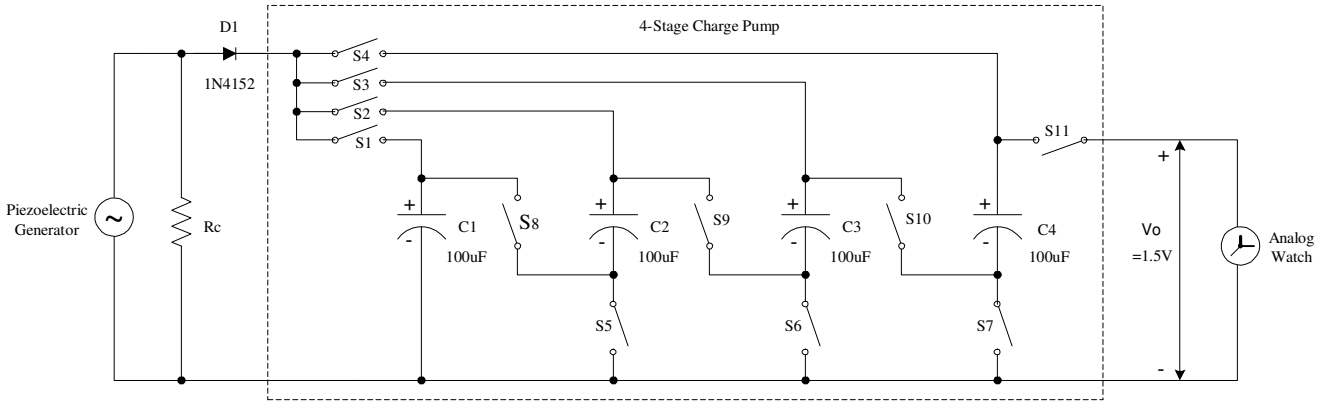


Fig. 1. Demonstration of completely passive proof-of-concept PCC for MPG.

composed of capacitors and MOSFETs, which both can be easily integrated on chip. The fact that the piezoelectric membrane is capacitive also makes a charge pump dc-dc converter more attractive.

A. Proof-of-Concept Demonstration

For the purpose of proof-of-concept demonstration, a totally passive PCC has been designed, as shown in Fig. 1. Diode D_1 rectifies the ac output of the P^3 engine. The 4-stage charge pump is operated manually through four toggle switches. The load is an analog wristwatch. At the beginning of the project, a polyvinyldifluoride (PVDF) membrane served as the piezoelectric generator. The 4-stage charge pump has two operation stages: first, aluminum electrolytic capacitors C_1~C_4 are arranged in parallel, and charged to 0.39V in about 2 minutes with no load; second, the four capacitors are connected in series to get 1.56V dc voltage, which runs the wristwatch for 5 seconds. Although the delivered power is very low, the simple demonstration does show that the system works. The resistor R_C helps to extract additional power from the piezoelectric membrane. Fig. 2 shows the relations between the capacitor charging time and capacitor terminal voltage at different R_C values. Four 100μF capacitors were charged to 1.0Vdc in parallel. Different R_C values were tested. The peak-to-peak output voltage of the piezoelectric generator is 2.09V. When R_C=45kΩ, the charging time is minimized, about 8.5 times less than the case without R_C.

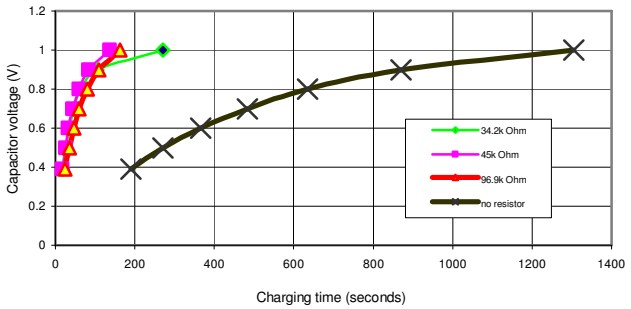


Fig. 2. The effect of Rc on the capacitor charging time.

B. Proposed Power Conditioning Circuit

At the current stage of the project, 21-layer lead zirconate titanate (PZT) membranes have been adopted as the piezoelectric generator. The output voltage of a single PZT membrane is in the range of 1.8~2.5V_{PP}. In this case, the diode rectifier's forward-voltage drop constitutes a significant fraction of the PZT output voltage. Even the commonly used Schottky diodes still have a relatively large voltage drop. Therefore, rectification is a nontrivial issue.

In this paper, synchronous rectification is employed to improve the PCC efficiency, as shown in Fig. 3. The comparator senses the source-drain voltage of the N-channel MOSFET. The MOSFET can only work in the third quadrant, i.e., it only conducts when the source of the MOSFET is positive with respect to its drain. The MOSFET body diode would not be forward-biased due to the very low on-state resistance R_{DS} of the MOSFET. When the drain of the MOSFET is positive with respect to its source, the body diode is reverse-biased.

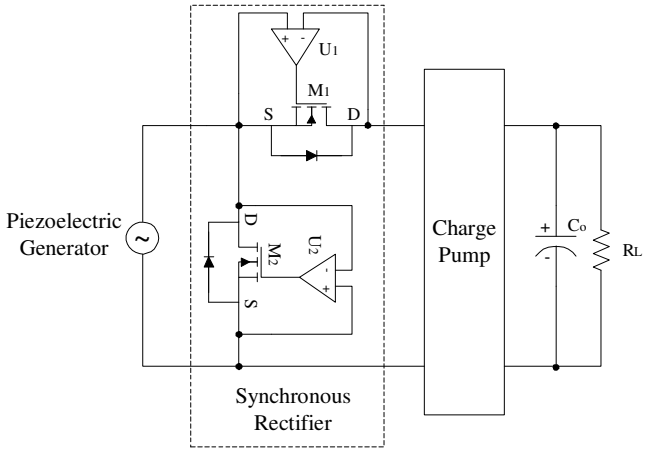
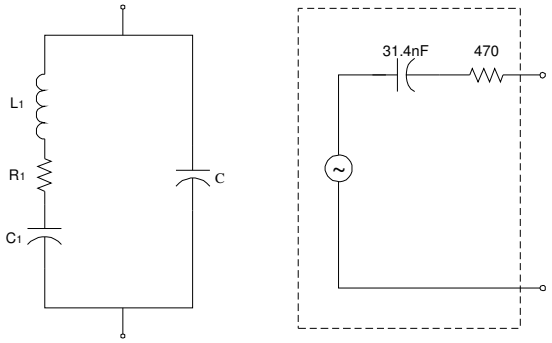


Fig. 3. Proposed PCC with synchronous rectification.

III. PSPICE SIMULATION

In this section, possible rectifier topologies in the PCC are simulated with PSpice. Fig. 4 (a) shows the commonly used Van Dyke's model for representing the equivalent circuit of a piezoelectric membrane. L_1, C_1, and R_1 are mass, elastic compliance and mechanical damping transformed into electrical magnitude by the piezoelectric effect, respectively. C_0 is the capacitance in the absence of mechanical deformation at the resonant frequency [11]. From the point-of-view of power extraction, the PZT should work at resonance. Therefore, instead of using Van Dyke's model in the simulation, a simplified model as shown in Fig. 4 (b) has been developed for PSpice simulation. The effectiveness of the simplified model will be verified in section V. By using this simplified model, PCC designers need not worry about the complex parameters of the piezoelectric generator. The parameters in the simplified model were obtained with an HP4284A Precision LCR Meter.



(a) Van Dyke's model (b) Simplified model

Fig. 4. Equivalent model of the piezoelectric generator.

In the PSpice simulation, in order to generate the same waveforms as a real P^3 cell, the harmonics of the PZT output waveform were computed with Matlab. The result is shown in Fig. 5. The 2^{nd} – 7^{th} harmonics were considered in the PSpice model.

Three schemes as shown in Fig. 6 are considered to be possible rectifier topologies and are compared in the simulation. Scheme I is taken from the proof-of-concept demonstration in Fig. 1. Scheme II replaces R_C in scheme I with a diode, looking like an ac-dc voltage doubler [12], which is shown in Fig. 7. The difference is that in scheme II, the inherent capacitance of the piezoelectric membrane is uncontrollable for PCC designers. Scheme III is the modified SR and is expected to further increase the extracted power from the piezoelectric generator. Fig. 8 shows the PSpice schematic and simulation waveforms for scheme III. Comparison of the simulation results for the three schemes is shown in Fig. 13. The PSpice simulation shows that the maximum extracted power with scheme II and scheme III are 225% and 412%, respectively, of that with scheme I.

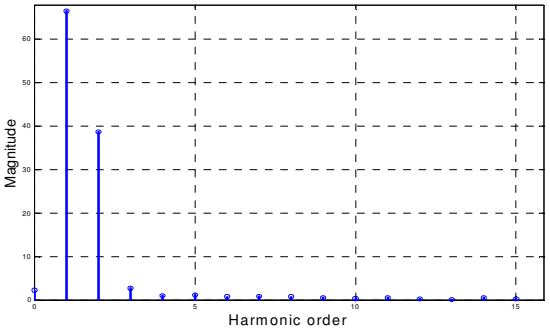
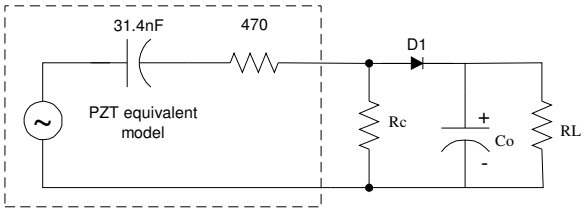
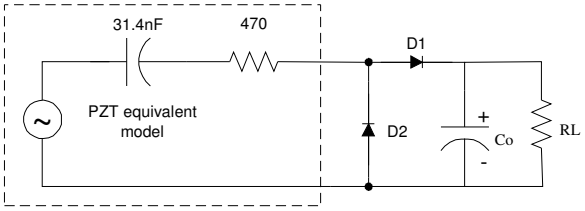


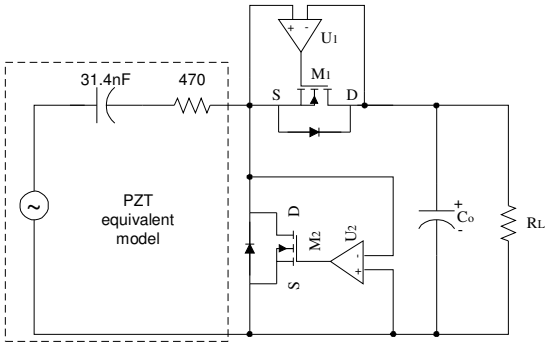
Fig. 5. FFT of an actual PZT output waveform.



(a) Scheme I: diode-resistor pair rectifier.



(b) Scheme II: diode-diode pair rectifier.



(c) Scheme III: modified synchronous rectifier.

Fig. 6. Possible rectification topologies

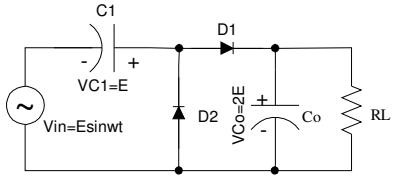
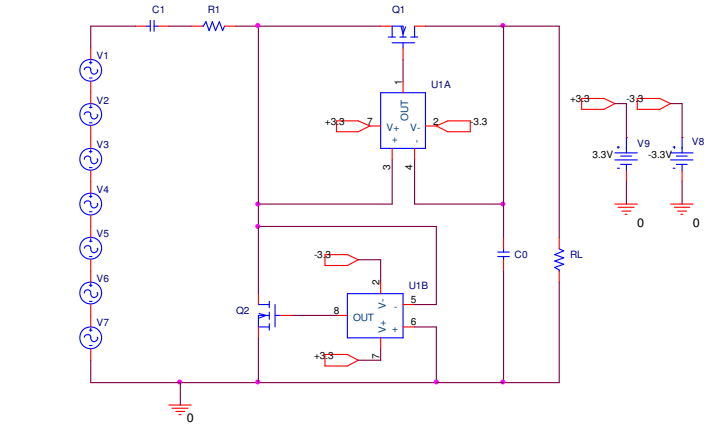
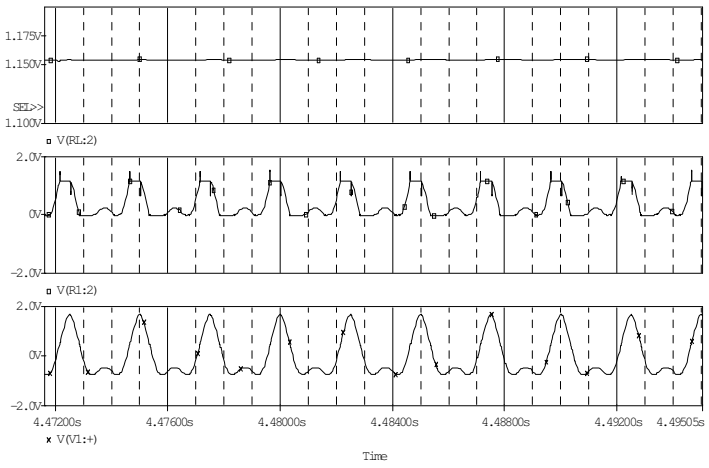


Fig. 7. An ac-dc voltage doubler.



(a) Schematic



(b) Simulation waveforms. Upper: dc output voltage; Middle: PZT output with load; Bottom: PZT output with no load

Fig. 8. PSpice simulation for scheme III.

IV. Experimental Setup

The experimental setup is shown in Fig. 9. It is based on the bulge tester and the PZT membranes provided by co-researchers at Washington State University. The bulge tester is used to simulate the action of the micro heat engine that drives the PZT membranes [13]. PZT membranes of different sizes are fabricated on a wafer. An actuator in the bulge tester provides the periodic mechanical excitation to the PZT membrane, which generates an ac voltage. The PCC then converts this ac voltage into the regulated dc voltage required by the load. The actuator is driven by a sine wave input in the range of -20Vac~120Vac, provided by a programmable source, in the Motor Systems Resource Facility (MSRF) at Oregon State University. A dc power supply is connected in series to the programmable source to provide the necessary offset. Fig. 10 shows the photos of the bulge tester and the wafer within its holder.

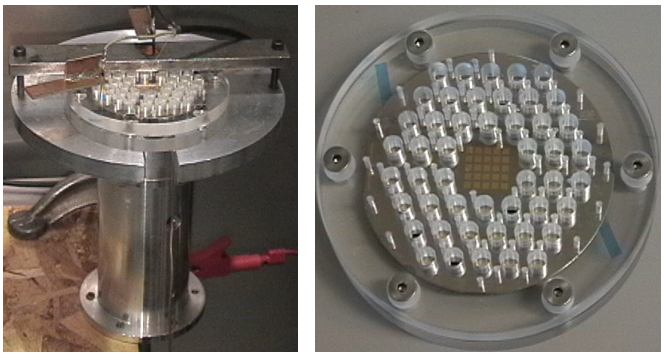


Fig. 10. Photos of (a) Bulge tester, and (b) Wafer and its holder.

V. Experimental Results And Discussion

The three rectification schemes in Fig. 6 were tested with the bulge tester. The PZT membranes' resonant frequency is about 400Hz. Fig. 11 (a) shows a typical PZT output voltage waveform at no load. Fig. 11 (b) and (c) shows the scheme III dc output voltage and PZT terminal voltage waveform, respectively, with a 70.6kΩ resistive load. The extracted powers at different loads for the three rectification schemes are shown in Fig. 13. From Fig. 13, it can be noted that scheme I can extract a maximum power of 3.7μW with an 80kΩ load. The maximum power extracted by scheme II and scheme III is 212% and 508% of that of scheme I, respectively. Also, in Fig. 13, the PSpice simulation results coincide very well with the test results of the bulge tester. Hence, the simplified model for the piezoelectric generator used in PSpice simulation is verified.

For scheme III, the power consumption of the comparators should not present a problem, since off-the-shelf comparators with a supply current of only 0.38μA are

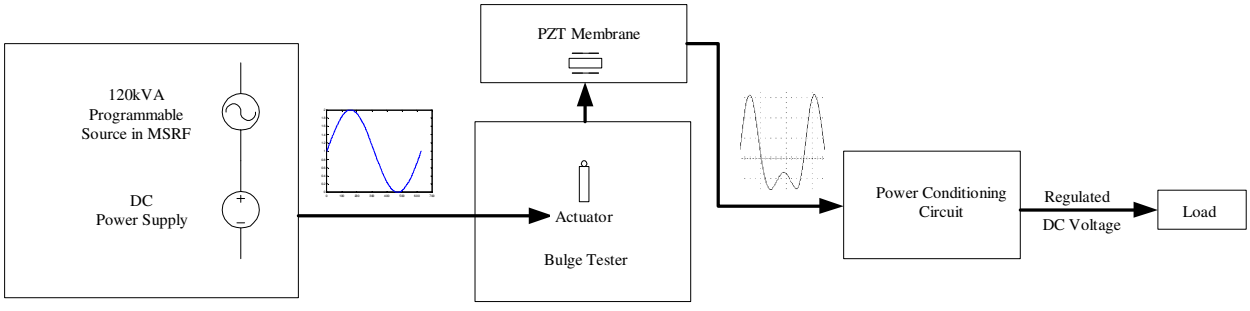
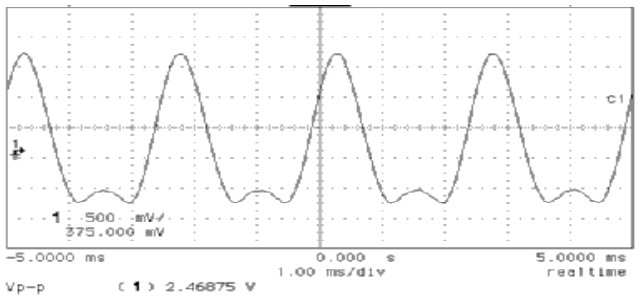
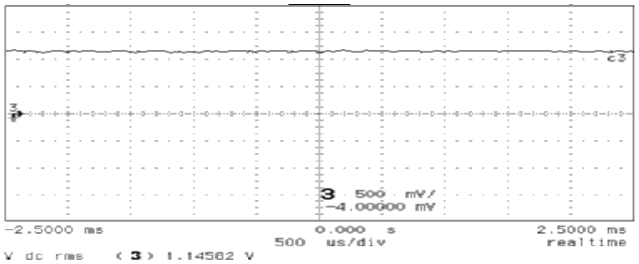


Fig. 9. Experimental setup.

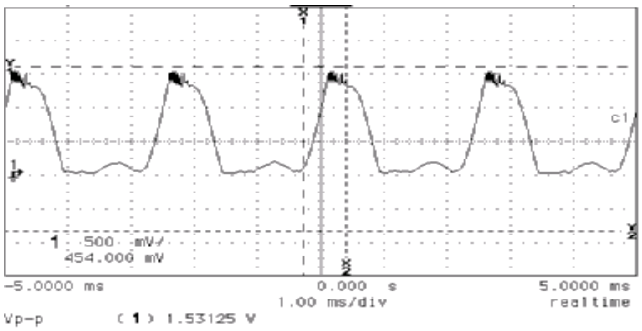
currently available. Considering this power consumption (3V, 2.28μW), the extracted power is still 447% of that of scheme I. In the future, with the PCC being integrated on a single chip, the comparator power consumption will be further decreased. A low power rechargeable "button-cell" battery can start up the circuit. During normal operation of the MPG, the battery will be trickle charged. In fact, scheme III has another potential advantage. A simple study on Fig. 6 (c) shows that the body diodes of the two MOSFETs have actually formed a diode-diode pair rectifier, i.e., scheme II. If there are no power supplies for the comparators, then scheme III will be degraded into scheme II, and there will still be dc output voltage. This voltage can then be regulated with on-chip charge pumps to drive the comparators, and scheme III will be activated, i.e., the circuit can be self-started. Therefore, it is possible to develop a totally passive PCC with scheme III.



(a) No load PZT output voltage waveform



(b) dc output voltage waveform with 70.6kΩ load



(c) PZT terminal voltage waveform with 70.6kΩ load

Fig. 11. PZT output waveforms from the bulge tester.

VI. Arbitrary Waveform Generator Representation Of The PZT Membrane

Since the power level of a single generator cell is very low, in order to achieve higher power, it is necessary to connect many cells in series or in parallel according to the load requirements. At the current stage of the project, it is obviously impractical to build many bulge testers for high power experiments. An alternative to the bulge tester is to develop a representative system with an arbitrary waveform generator and the necessary interfacing circuits.

An arbitrary waveform generator representation (AWGR) of a generator cell has been developed, as shown in Fig. 12. The interface circuit is obtained with the PZT impedance parameters. The actual waveform of a P^3 cell is transferred to the arbitrary function generator AFG310 via GPIB cable. All three rectifier schemes were studied with the AWGR, and the results are again shown in Fig. 13 for comparison. Fig. 13 shows that the AWGR test results are very close to that of the bulge tester. Fig. 14 shows some waveforms for scheme III with an 80kΩ load. The terminal voltage and current of the interface circuit can be measured to calculate the input power of the PCC. Therefore, the rectifier efficiency can be evaluated. The efficiency of scheme III is approximately 92% with an 80kΩ resistive load. The efficiency of scheme II is only 68% with the same load. Compared to the bulge tester, the AWGR is programmable, flexible, more robust, and easier to operate. Therefore, tests can be performed on the AWGR, rather than directly on the bulge tester. For example, a P^3 engine has been stacked with the AWGR in series. After the PZT and AWGR were synchronized, i.e., acquired the same frequency and phase, their outputs were added up successfully. This experiment shows the feasibility of cascading many P^3 engines in the future to achieve increased output power.

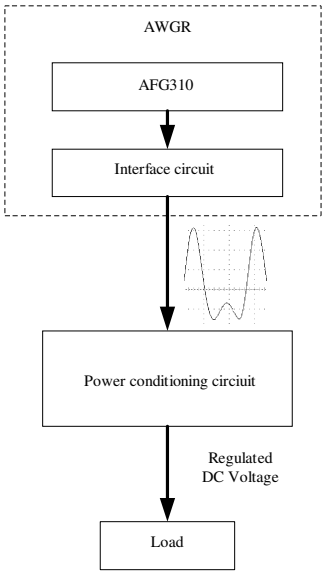


Fig. 12. Schematic of the AWGR.

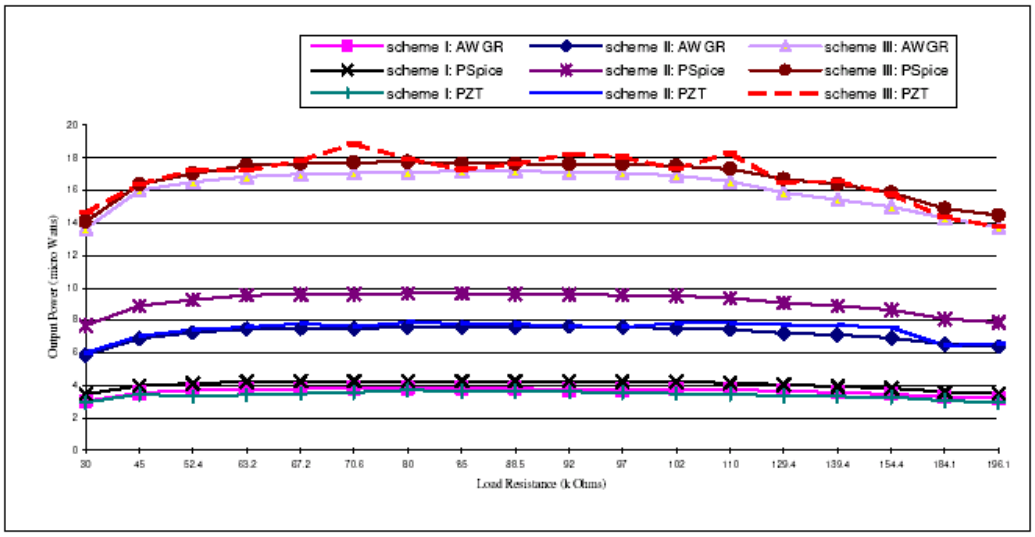


Fig. 13. Comparison of PSpice simulation, bulge tester and AWGR test results for the three rectifier schemes.

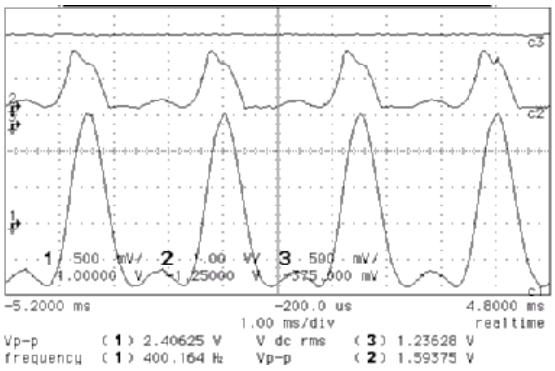


Fig. 14. AWGR waveforms. Upper: dc output voltage with 80kΩ load; Middle: AWGR terminal voltage with 80kΩ load; Bottom: AWGR terminal voltage with no load.

VI. Conclusions And Future Work

Low power devices promote the development of micro power generators (MPGs). A novel power conditioning circuit (PCC) is proposed to extract maximum power from an MPG, using synchronous rectification (SR) technology applied to the primary side of the PCC. Proof-of-concept demonstration includes a 4-stage completely passive charge pump driving an analog wristwatch, proving proper operation of the entire P^3 micro power system. A simplified model of the piezoelectric generator is developed and verified through PSpice simulation. Performance of the proposed PCC is also verified by PSpice simulation as well as experimentally. A maximum output power of 18.8μW can be extracted from a single piezoelectric MPG, with a PCC efficiency of 92%. Arbitrary waveform generator representation (AWGR) of the piezoelectric membrane is also presented. AWGR facilitates future tests and demonstrates the feasibility of cascading many MPGs to achieve increased output power. Future work will include integrating the PCC on a single chip.

Acknowledgements

The financial support for this project was provided by the Defense Advanced Research Projects Agency (DARPA).

References

[1] F. Moll, and A. Rubio, "Human Powered Piezoelectric Batteries to Supply Power of Wereables Electronic Devices," Int. J. Soc. Mater. Eng. Resour., Vol. 10 No 1 Mar. 2002, pp 34-40.

[2] http://www.darpa.mil/mto/mpg/overview/index.html, "Micro Power Generation: Overview".

[3] N. S. Shenck, et al, "Energy Scavenging with Shoe-Mounted Piezoelectrics," IEEE Micro, Vol. 21, No.3, May/June 2001, pp.30-42.

[4] T. Starner, "Human Powered Wearable Computing," IBM Syst. J., vol.35, nos. 3/4, 1996, pp.618-629.

[5] S. Meninger, et al, "Vibration-to-Electric Energy Conversion", IEEE Trans. VLSI Systems, Vol. 9, 2001, pp. 64-76, 2001.

[6] F. Moll, and A. Rubio, "An approach to the analysis of wearable body-power system," MIXDES 2000, June 2000.

[7] S. Horowitz, et al, "Technology Development for Self-Powered Sensors," AIAA Paper 2002-2702, the 1st Flow Control Conference, June 2002.

[8] G. K. Ottman, et al, "Adaptive Piezoelectric Energy Harvesting Circuit for Wireless Remote Power Supply," IEEE Trans. on Power Electronics, vol. 17, No. 5, Sep. 2002, pp.669-676.

[9] S. Whalen, et al., "Design, Fabrication and Testing of the P3 Micro Heat Engine," Sensors and Actuators, In Press, Jan. 2003.

[10] N. Mohan, et al, Power Electronics Converters, Applications, and Design, 2nd ed., John Wiley & Sons. INC., New York, 1995.

[11] B. Jaffe, W. R. Cook, and H. Jaffe, Piezoelectric Ceramics, Academic Press, London, 1971.

[12] P. M. Lin and Leon O. Chua, "Topological Generation and Analysis of Voltage Multiplier Circuits," IEEE Trans. on Circuits and Systems, Vol. CAS-24, No. 10, Oct. 1977, pp517-530.

[13] J. D. Hall, N. E. Apperson, B. T. Crozier, C. Xu, R. F.Richards, D. F. Bahr, and C. D. Richards, "A Facility for Characterizing the Dynamic Mechanical Behavior of Thin Film Membranes for Microelectromechanical Systems", Review of Scientific Instruments, Vol. 73, pp. 2067-2072, 2002.

A New Approach to Reducing Output Ripple in Switched-Capacitor-Based Step-Down DC/DC Converters

Jifeng Han, Annette von Jouanne, Alan K. Wallace, Gabor C. Temes
School of Electrical Engineering and Computer Science
Oregon State University
Corvallis, OR 97331-3211
Tel: 541-737-0831, Fax: 541-737-1300
avj@ece.orst.edu

Abstract – **Rapidly dropping power supply voltages and tight voltage regulation requirements for integrated circuits challenge power supply designers. A novel interleaved discharge (ID) approach is proposed to reduce the output ripple in step-down switched-capacitor (SC) dc-dc converters. The proposed ID approach provides flexibility in optimizing the design of SC dc-dc converters.**

I. INTRODUCTION

Power supply voltages for integrated circuits (ICs) are being reduced steadily in an effort to increase integration densities and reduce power dissipation. According to [1], the 2002 "International Technology Roadmap for Semiconductors", by 2016, the supply voltage for high performance ICs will drop to only 0.4V. Along with the plummeting supply voltages, the currents drained by ICs are going to be much higher due to increasing power requirements. This trend presents power supply designers with many tough challenges, such as supply efficiency, regulation, ripple, response time, size/weight, cost, power bus architecture, etc, [2], [3]. In applications such as computers, a higher voltage (e.g., 12V) is more suitable for efficient power delivery, because of reduced resistive losses in the copper traces on printed circuit boards. The voltage delivered on-board needs to be converted into required supply voltages through voltage regulator modules (VRMs) [4]. Therefore, for future low-voltage applications, step-down (buck) dc-dc converters are becoming important. In conventional switch-mode power supplies (SMPSs), due to the use of magnetic components (inductor and transformer), it is difficult to achieve high power density and low cost designs.

In recent years, switched-capacitor (SC) dc-dc converters (also known as charge pumps) have gained increased attention [5]-[8]. There have already been many commercial products in use [9], [10]. The increasing popularity of SC dc-dc converters is mainly due to their unique features: they consist of only switches and capacitors, and energy transfer is achieved by controlling the charging and discharging process of the capacitors. Because no magnetic components are needed, SC dc-dc converters are amenable to single chip integration.

Thus far, the output ripple issues in SC dc-dc converters have only received limited attention. In SMPSs, the percentage output voltage ripple is usually specified to be less than 1% [11]. The value of the output capacitance can be simply increased to meet the ripple specification, but this method may not meet low-cost and high-power density design requirements. Interleaving techniques have already been used in low-voltage high-current SMPSs to improve the power level [12]-[14], as shown in Fig. 1. The N converter cells are physically paralleled and operated at the same switching frequency, but are phase-shifted by $2\pi/N$ with respect to one another. By interleaving N-paralleled converter cells, the input/output ripple can be reduced by 1/N or more. The cost of this interleaving technique is increased component count and complicated control. Interleaving technique has also found its use in SC dc-dc converters to reduce output ripple [7], [10].

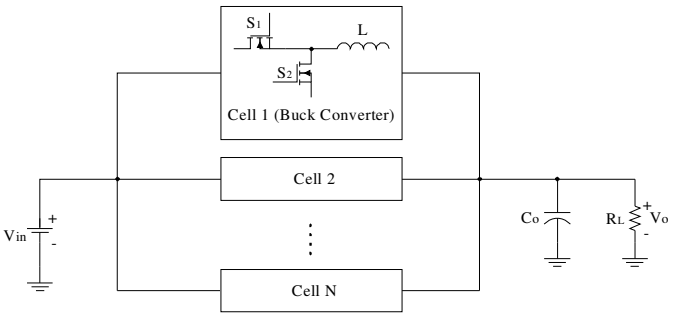


Fig.1. Interleaving technique

In this digest, conventional step-down SC dc-dc converters are first reviewed, after which a new approach to reducing the output ripple is proposed, taking full advantage of the structure of step-down SC dc-dc converters. In Section III, the proposed approach is analyzed using state-space averaging. Simulation results are provided in Section IV to demonstrate the effectiveness of the proposed approach. Experimental results are being pursued and will be included in the final paper.

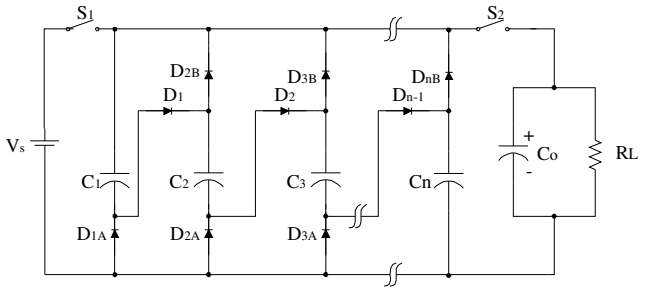
II. PROPOSED INTERLEAVED DISCHARGE APPROACH

A. Conventional Step-Down SC dc-dc Converter

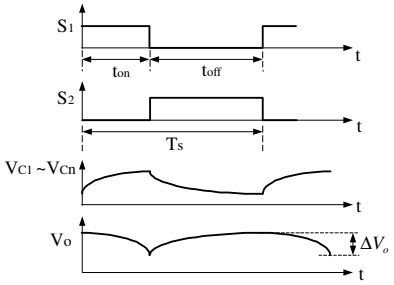
Fig. 2 (a) shows the schematic of a conventional n-stage step-down SC dc-dc converter. Its timing diagram and some theoretical waveforms are shown in Fig. 2(b). In each switching cycle, the circuit goes through two different switching states. During t_{on}, capacitors C_1~C_n (called pump

capacitors) are charged in series through S_1, and D_1 to D_{n-1}. The output capacitor C_o supplies the load during this interval. During t_{off}, the pump capacitors are connected in parallel through diodes D_{1A} ~ D_{n-1A} and D_{2B} ~ D_{nB}, so that they can be discharged simultaneously to the load through S_2. The output voltage is ideally

$$V_o = \frac{V_s}{n} \quad (1)$$



(a) Circuit

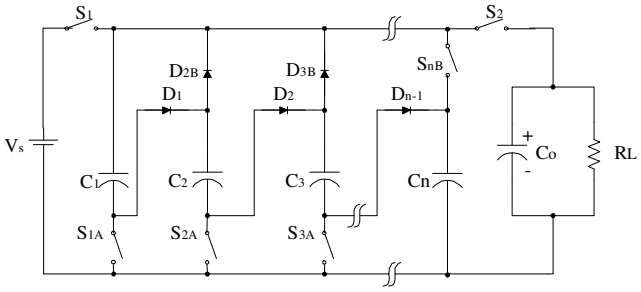


(b) Timing diagram and waveforms

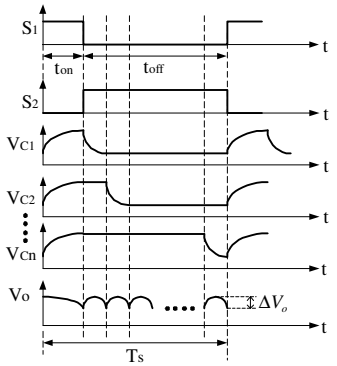
Fig. 2. Conventional n-stage step-down SC dc-dc converter

B. Proposed Step-Down SC dc-dc Converter with Interleaved Discharge

The proposed n-stage step-down SC dc-dc converter is shown in Fig. 3 (a). Unlike in a conventional step-down SC dc-dc converter where the pump capacitors are discharged simultaneously, in the proposed SC dc-dc converter the pump capacitors are discharged one by one, which is here termed interleaved discharge (ID). To realize interleaved discharge of the pump capacitors, diodes D_{1A}~D_{n-1A} and D_{nB} in Fig. 2 (a) are replaced by power switches. For an n-stage step-down SC dc-dc converter, the interleaved discharging process is realized by introducing a phase shift of $2\pi/n$ to each pump capacitor during the discharging interval. Therefore, by applying the ID method we could obtain an output ripple with a frequency of nT_S. Because the output voltage ripple is inversely proportional to the ripple frequency, the output ripple can be reduced by n times. Fig. 3 (b) shows the timing diagram and waveforms for the proposed SC dc-dc converter. It can be seen that while C_1 is being discharged, other capacitors are kept untouched, i.e., their voltages don't change. The similar process is repeated to other capacitors till the end of t_{off}. Compared to Fig. 2 (b), the output voltage V_O in Fig. 3 (b) has higher frequency and reduced peak-peak ripple, with the same capacitors. Fig. 4 shows the circuit configuration during different switching states. Discharging intervals 2~n are similar to Fig. 4 (b), except include a phase shift of $2\pi/n$.

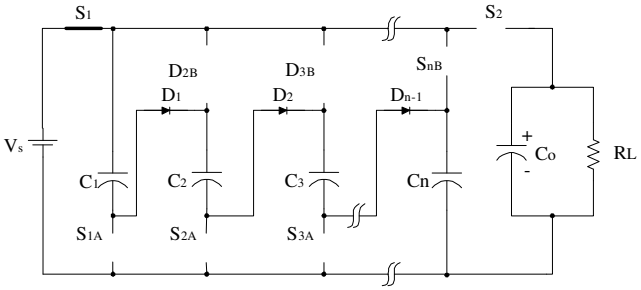


(a) Circuit

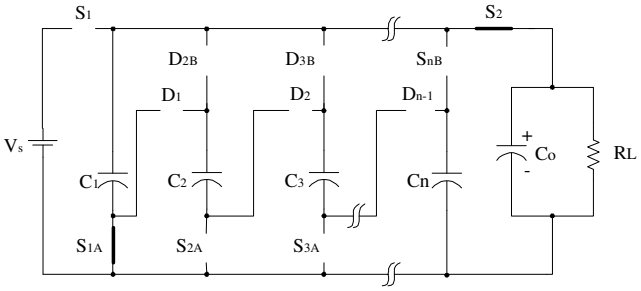


(b) Timing diagram and waveforms

Fig. 3. Proposed step-down SC dc-dc converter with interleaved discharge



(a) Charging interval



(b) Discharging interval 1

Fig. 4. Circuit configuration of the proposed step-down SC dc-dc converter during different switching states

The proposed ID method is also a kind of interleaving technique. However, it is different from the conventional interleaving technique as already shown in Fig. 1. The ID method takes full advantage of the special structure of the step-down SC dc-dc converters, and it does not need any extra converter cells. The ID method does need some extra driving signals for the switches, but simple circuits such as flip-flops can be used.

It should be pointed out that the power switches (in Fig. 3(a)) that replace the original diodes (in Fig. 2(a)) would not present difficulties since it is possible to integrate power switches on chip in low-power applications. In order to obtain high efficiency in low-voltage low-power applications, all of the diodes should be replaced by power switches. Also, floating diodes are difficult to realize in CMOS. For medium-power conventional SC dc-dc converters, replacing the diodes with power switches can still improve the efficiency. The ID method can be applied to any step-down SC dc-dc converters.

III. STEADY-STATE ANALYSIS

Fig. 5 shows a step-down SC dc-dc converter that was proposed in [5]. As can be seen from Fig. 5, this circuit has employed the interleaving technique, i.e., two identical cells work in antiphase. Since the ID method can be applied to any step-down SC dc-dc converters, the converter in Fig. 5 is here used as an example to analyze the steady-state performance of the proposed ID approach (see Fig. 6). In Fig. 6, switches S_5 to S_8 replace the original diodes D_1, D_3, D_4, and D_6 in Fig. 5. Suppose the diodes are replaced with switches that also have a voltage drop of V_d, so that we can make a fair comparison of the steady-state output voltages of the converters in Fig. 5 and Fig. 6. The steady-state output voltages in Fig. 5 are as follows [5]

$$V_o = \frac{V_s - 3V_d}{2 + \frac{1}{R_L}[(2r_2 + r) + \frac{2r + r_1}{4D}]} \qquad (2)$$

Here, r represents the equivalent series resistance (ESR) of capacitors C_1~C_4, r_1 is the on-resistance of S_1 and S_3, and r_2 for S_2 and S_4.

The converter in Fig. 6 is analyzed using state-space averaging [15]. Suppose the charging time t_{on} is less than $T_s/4$, and then there will be a total of six switching states. Let the state variables represent the voltages of capacitors C_1~C_4 and C_o. Thus, the state equations for each switching state is

$$\dot{X}(t) = A_k X(t) + B_k U\,, \qquad \text{k=1,2…6} \qquad (3)$$

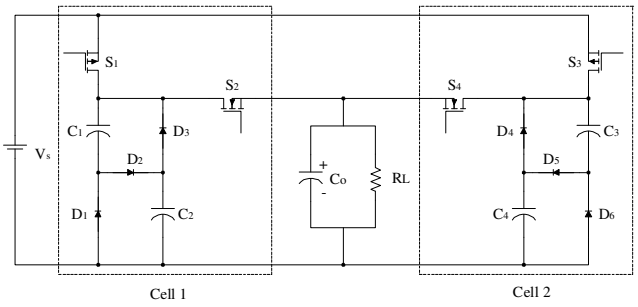
Where

$$X = [V_{C1} \quad V_{C2} \quad V_{C3} \quad V_{C4} \quad V_{Co}]^T = [x_1 \quad x_2 \quad x_3 \quad x_4 \quad x_5]^T$$

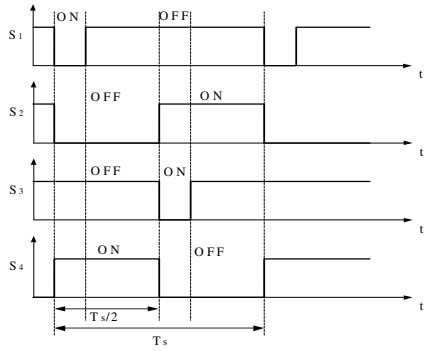
$$U = [V_s \quad V_d]^T$$

Finally, the average state equation is

$$\dot{X}_{av}(t) = A_{av} X_{av}(t) + B_{av} U = \sum_k d_k A_k X(t) + \sum_k d_k B_k U \qquad (4)$$

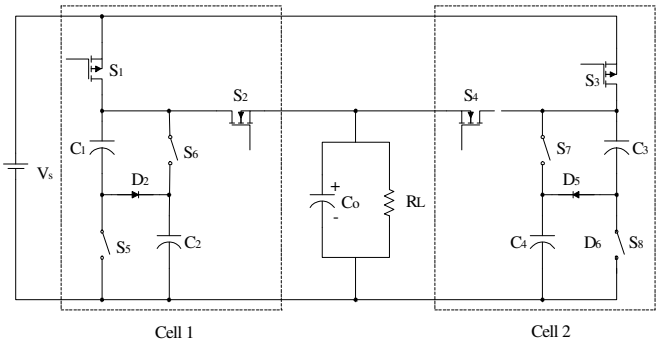


(a) Circuit

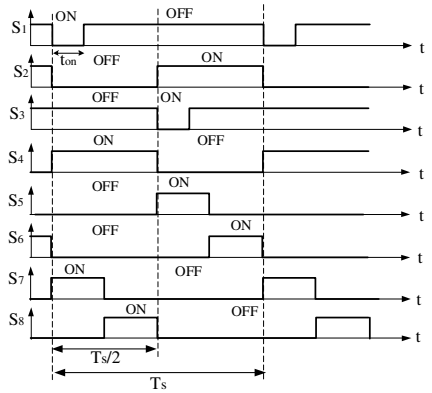


(b) Timing diagram

Fig. 5. Step-down SC dc-dc converter proposed in [5]



(a) Circuit



(b) Timing diagram

Fig. 6. Proposed ID method applied to the converter in Fig. 5.

Where the weight d_k denotes the ratio of each switching interval t_k to the switching period T_s.

To get the steady-state output voltage expression, we let $\dot{X}_{av}(t) = 0$, therefore $X_{av}(t) = -A_{av}^{-1} B_{av} U$ (5)

The state equations for each of the switching states can be obtained following the similar method in [5]. After that, the matrices in the average state equation are obtain as follows

$$A_{av} = \begin{bmatrix} -\frac{Dg_1}{C} - \frac{g_2}{4C} & -\frac{Dg_1}{C} & 0 & 0 & \frac{g_2}{4C} \\ -\frac{Dg_1}{C} & -\frac{Dg_1}{C} - \frac{g_2}{4C} & 0 & 0 & \frac{g_2}{4C} \\ 0 & 0 & -\frac{Dg_1}{C} - \frac{g_2}{4C} & -\frac{Dg_1}{C} & \frac{g_2}{4C} \\ 0 & 0 & -\frac{Dg_1}{C} & -\frac{Dg_1}{C} - \frac{g_2}{4C} & \frac{g_2}{4C} \\ \frac{g_2}{4C_o} & \frac{g_2}{4C_o} & \frac{g_2}{4C_o} & \frac{g_2}{4C_o} & -\frac{g_2}{C_o} - \frac{Y}{C_o} \end{bmatrix}$$

$$B_{av} = \begin{bmatrix} \frac{Dg_1}{C} & -\frac{Dg_1}{C} + \frac{g_2}{4C} \\ \frac{Dg_1}{C} & -\frac{Dg_1}{C} + \frac{g_2}{4C} \\ \frac{Dg_1}{C} & -\frac{Dg_1}{C} + \frac{g_2}{4C} \\ \frac{Dg_1}{C} & -\frac{Dg_1}{C} + \frac{g_2}{4C} \\ 0 & -\frac{g_2}{C_o} \end{bmatrix} \quad (6)$$

Applying (5), we then obtain the steady-state output voltage as

$$V_o = \frac{V_s - 3V_d}{2 + Y_L(\frac{2}{g_2} + \frac{1}{4g_1 D})} = \frac{V_s - 3V_d}{2 + \frac{1}{R_L}[2(r_2 + r) + \frac{2r + r_1}{4D}]} \quad (7)$$

The only difference between (7) and (2) is that the second factor in the denominator of (7) contains one more ESR. Since $r/R_L \ll 1$, the steady-state output voltage of the ID-based charge pump is very close to that of [5]. Therefore, the efficiency of the ID-based SC converter should be very close to that of the conventional one, which means that the ID method does not sacrifice the converter efficiency.

IV. VERIFICATION BY SIMULATION

In [6], a 48W, 55V/12V switched-capacitor dc-dc converter was proposed, as shown in Fig. 7. In this section, the proposed ID method is applied to this converter. Fig. 8 illustrates the PSpice simulation waveforms without using the ID method. Fig. 9 shows the PSpice simulation waveforms using the proposed ID method. Note that in Fig. 8 (a) to (c) the voltage waveforms of C_2 to C_4 are in phase, which is the feature of conventional step-down SC dc-dc converters. In Fig. 9 (a) to (c), a phase shift exists in the voltage waveforms of C_2 to C_4. After using the proposed ID method, the output ripple (Fig. 9 (d)) is much smaller than that of a conventional step-down SC dc-dc converter, as shown in Fig. 8 (d).

The simulation results of both cases are tabulated in Table 1. It is shown that the proposed ID method can reduce the output ripple by a factor of 3, without sacrificing the converter efficiency. Thus, the effectiveness of the proposed ID method is verified by simulation.

TABLE 1 SIMULATED PERFORMANCE COMPARISONS OF A STEP-DOWN SC DC-DC CONVERTER WITH AND WITHOUT ID APPROACH

	Average Output voltage (V)	Average Input current (A)	Efficiency (%)	Output Ripple (mV)
In [6] (without ID)	11.98	1.0015	Not given *	94
This work (with ID)	11.94	1.008	85.70	24

* In [6], the provided theoretical efficiency was 87.2%, and the experimental efficiency was 82.3%.

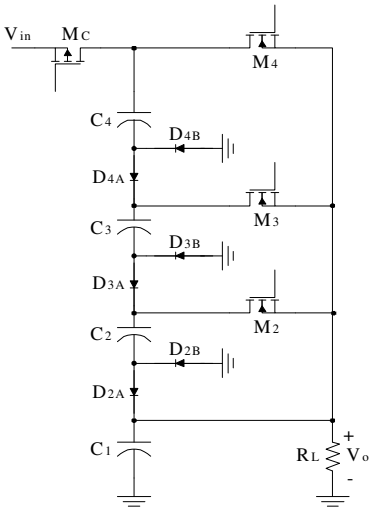


Fig. 7. Four-stage SC dc-dc converter proposed in [6]. C_2=C_3=C_4=9.6μF, C_1=86.4μF, R_L=3Ω, V_{in}=55V, V_o=12V, f_s=100kHz.

V. CONCLUSIONS

In this digest, an interleaved discharge (ID) approach was proposed to reduce the output ripple in switched-capacitor-based step-down dc-dc converters. The proposed ID approach takes full advantage of the structure of step-down SC dc-dc converters. The steady-state performance of the proposed step-down SC dc-dc converter was analyzed using state-space averaging. Simulation of a four-stage SC dc-dc converter shows that the ID approach can reduce the output ripple by a factor of 3, without sacrificing the converter efficiency. The proposed ID approach is suitable for any step-down SC dc-dc converter.

The proposed ID approach not only provides the possibility to reduce the output ripple, but also provides some flexibility in optimizing the design of step-down SC dc-dc converters. Considering the fact that the proposed ID approach effectively increases the ripple frequency, it is not difficult to conclude that the ID approach can be used for other benefits: if the output ripple is kept constant, we can reduce the capacitance value of the output filter for lower cost and higher power density, or reduce the switching frequency for higher efficiency due to reduced switching losses. Experimental results are currently being pursued and will be included in the final paper.

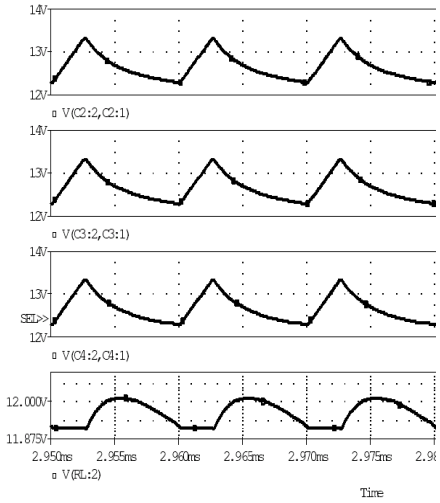


Fig. 8. Simulation waveforms without interleaved discharge (ID). (a)~(c) Voltages of C_2~C_4, (d) Output voltage

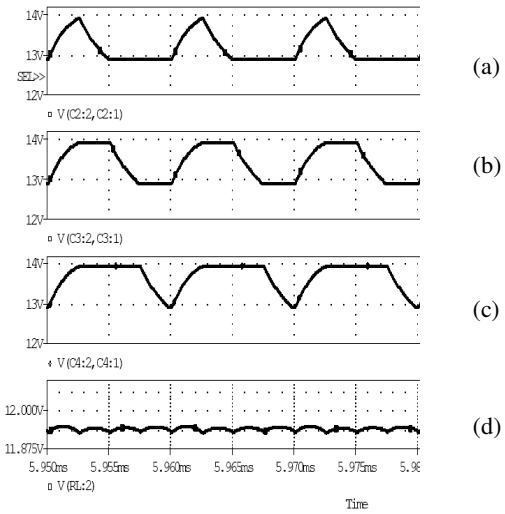


Fig. 9. Simulation waveforms with interleaved discharge (ID). (a)~(c) Voltages of C_2~C_4, (d) Output voltage

REFERENCES

[1] http://public.itrs.net/Files/2002Update/Home.pdf, "International Technology Roadmap for Semiconductors 2002 Update."

[2] Ionel Dan Jitaru, "Future Embedded Computer Systems Will Face Power Supply Design Challenges," *PCIM*, July 2000.

[3] Randhir Malik, "Future Embedded Computer Systems Will Require a New Power Bus Architecture," *PCIM*, July 2000.

[4] http://www.intel.com/design/Xeon/guides/29864601.pdf, "VRM 9.1 DC-DC Converter Design Guidelines."

[5] S. V. Cheong, et al, "Inductorless DC-to-DC Converter with High Power Density," *IEEE Trans. on Industrial Electronics*, vol. 41, No. 2, April 1994, pp. 208-215.

[6] W. S. Harris, and K. D. T. Ngo, "Power Switched-Capacitor DC-DC Converter: Analysis and Design," *IEEE Trans. on Aerospace and Electronic Systems*, vol. 33, No. 2, April 1997, pp. 386-395.

[7] Seung-Chul Lee, et al, "A Low-Ripple Switched-Capacitor DC-DC up Converter for Low-Voltage Applications," *ASICs, Proceedings of the Second IEEE Asia Pacific Conference on*, 28-30 Aug., 2000, Page(s): 13 –16.

[8] Henry S. H. Chung, et al, "Development of Low-Profile DC/DC Converter Using Switched-Capacitor Circuits and Coreless PCB Gate Drive," *Power Electronics Specialists Conference*, vol. 1 , 27 June-1 July 1999, pp. 48 –53.

[9] http://pdfserv.maxim-ic.com/arpdf/ICL7660-MAX1044.pdf.

[10] National Semiconductor Corporation, "LM2781 Ultra-Low Ripple Switched Capacitor Voltage Inverter."

[11] N. Mohan, et al, Power Electronics Converters, Applications, and Design, 2nd ed., John Wiley & Sons. INC., New York, 1995.

[12] Chin Chang, and Mike A. Knights, "Interleaving Technique in Distributed Power Conversion Systems," *IEEE Trans. Circuit and Systems*, vol. 42, No., 5, May 1995, pp. 245-251.

[13] Peng Xu, et al, "A Family of Novel Interleaved DC/DC Converters for Low-Voltage High-Current Voltage Regulator Module Applications," *Power Electronics Specialists Conference*, vol. 3, June 2001, pp. 1507 – 1511.

[14] D. J. Perreault, and J. G. Kassakian, "Distributed Interleaving of Paralleled Power Converters," *IEEE Trans. Circuit and Systems*, vol. 44, No., 8, Aug. 1997, pp. 728-734.

[15] R.D. Middlebrook, and S. Cuk, "A General Unified Approach to Modeling Switching-Converter Power Stages," *IEEE Power Electronics Specialists Conference Record*, June 1976, pp. 18-34.

Design of an SRM-Based Actuator for High-Performance Steering Vane Control on the Landing Craft Air Cushion (LCAC) Hovercraft

Jifeng Han, Xiaolin Zhou, Annette von Jouanne, Alan Wallace
School of Electrical Engineering and Computer Science
Oregon State University
Corvallis, OR 97331 USA

Dallas Marckx, Greg Hjelmeland
Chinook Power Technologies, LLC
25977 SW Canyon Creek Road, Suite G
Wilsonville, OR 97070 USA

Jerry Lloyd, Pete Wung
Emerson Motor Company
8100 W. Florissant
St. Louis, MO 63136

Abstract – This digest presents a switched reluctance motor (SRM) based actuator for use on the landing craft air cushion (LCAC), to replace the existing hydraulic systems that control the steering vanes. The proposed SRM-based actuator enables the reduction of complexity, weight, and maintenance associated with conventional hydraulic systems. The proposed actuator consists of an SRM and a high-efficiency screw with suitable mechanical advantage. A preliminary SRM is designed with an analytical method, and then verified with an SRM design package – the Switched Reluctance Design and Simulation (SRDaS) program. A proof-of-concept demonstration has been set up to show the basic functionality of the proposed SRM-based actuator. Future work includes investigating the application of high-flux-density lamination materials as well as optimized operational speeds and dimensions of the SRM design.

I. INTRODUCTION

Recently, the U.S. Navy concept of the all-electric ship (AES) has gained increased attention [1]-[3]. Some of the important benefits of an AES include [1], [2]:

- Improved performance
- Reduced complexity and weight
- Reduced maintenance costs
- Reduced signatures
- Increased survivability

In keeping with the Navy's efforts to develop AESs, this digest presents a switched reluctance motor (SRM) based actuator for use on the U.S. Navy landing craft air cushion (LCAC). The proposed actuator will be used to replace the existing hydraulic systems that control the steering vanes of the LCAC. The conventional hydraulic systems, as shown in Fig. 1, need frequent costly maintenance.

To realize the required linear motion, the proposed actuator consists of an SRM drive and a roller-screw, which is connected to the rotor of the SRM. The function of the screw is twofold. First, it converts the rotational motion of the SRM rotor into linear motion required by the rudder control. Second, it provides suitable mechanical advantage for the actuator. Insufficient mechanical advantage will lead to impractical motor size and weight. An SRM is chosen because of its simple structure, ruggedness, and fault-tolerance capabilities [4]. Compared to other electric motors, an SRM also features high power densities. The proposed SRM-based actuator enables the reduction of complexity, weight, and maintenance associated with conventional hydraulic systems.

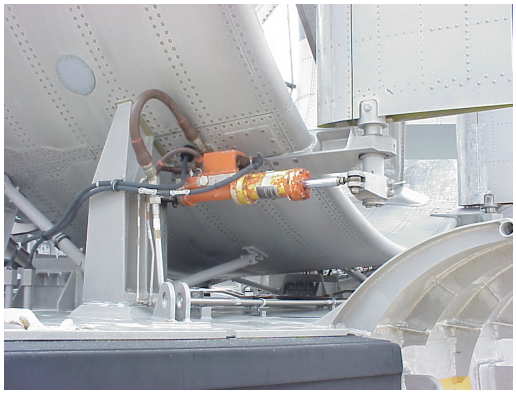


Fig. 1. Conventional hydraulic steering vane control system of the LCAC.

This digest is arranged as follows: in Section II, a preliminary SRM is designed with an analytical method, which is then verified with the Switched Reluctance Design and Simulation (SRDaS) program. Section III presents the sensorless controller design. A proof-of-concept demonstration is provided in Section IV to show the basic functionality of the proposed

actuation system. Section V summarizes the digest. Experimental results for the fully scaled actuator will be included in the final paper, as well as the investigation of high-flux-density lamination materials and optimized operational speeds and dimensions of the SRM design.

II. DESIGN OF THE SRM

Two techniques are combined to design the SRM. First, the analytical method introduced in [5] is used to give a relatively quick preliminary design. Then, SRDaS is employed, using finite element analysis, to verify and refine the preliminary design.

A. Actuator Specifications

The specifications of the actuator are listed in Table 1. Note that the total weight of the actuator is a key design parameter. Based on the specifications given in Table 1, the minimum output power of the SRM can be easily calculated, as shown in Table 2. This work focuses on the popular 4-phase, 8/6 machine, which was chosen from consideration of its fault-tolerance capability, converter complexity, and system efficiency.

TABLE 1 ACTUATOR SPECIFICATIONS

Parameter	Value
Input AC voltage -- 3 phase, line-to-line, rms	200 V
Input frequency	400 Hz
Stroke	5.6 inch
Speed	5.5 inch/sec
Total weight	≤12 lbs
Operating thrust	1100 lbs

TABLE 2 CALCULATION OF THE MINIMUM OUTPUT POWER OF THE SRM

Parameter	Value
Pitch of thread of the screw	0.25 inch
Screw efficiency	0.80
Screw diameter	1.00 inch
Mechanical advantage of the screw	10.05
Force applied to the screw	109.42 lbs
Motor output torque	54.71 lb-inch = 6.18 Nm
Screw revolutions per full stroke	20.40
Rotational speed of screw	22.00 rev/sec = 1320 rpm
Angular speed of screw	138.23 rad/sec
Motor min. output power	1.15 hp

B. Preliminary SRM design with analytical method [5]

In [5], Praveen presented a step-by-step analytical procedure for designing SRMs. In this subsection, a preliminary SRM is designed with this method. The main parameters of the preliminary design are tabulated in Table 3. The relationship between the flux linkage and phase current is shown in Fig. 2.

TABLE 3 MAIN PARAMETERS OF THE PRELIMINARY SRM

Parameter	Value
Rated torque	6.2 Nm
Rated speed	1320 rpm
Stator outer radius	71 mm
Rotor outer radius	33.5 mm
Shaft length	181 mm
Stack length	55 mm
Air gap	0.25 mm
Number of windings	166
Aligned inductance	18.2 mH
Unaligned inductance	4.2 mH
Total weight of the motor	11 lbs

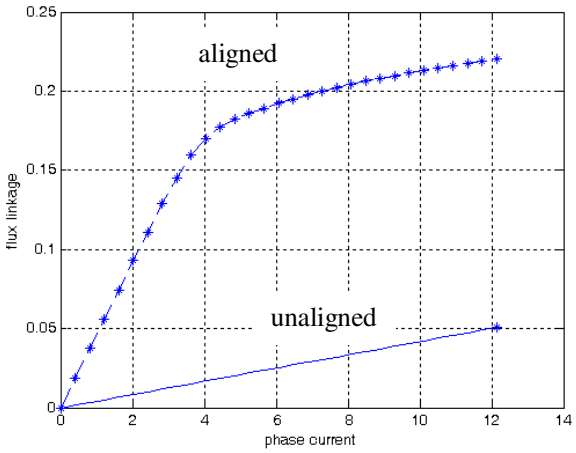


Fig. 2. Plot of Flux Linkage vs. Current for the Preliminary Design.

C. Verification of the SRM design with SRDaS [6]

In this subsection, SRDaS, developed by Rasmussen [6], is employed to verify the above designed SRM. The finite element method (FEM) is used in SRDaS. All of the parameters of the SRM are directly taken from the preliminary design. Fig. 3 shows the design interface in SRDaS. The plots of flux linkage vs. current and static torque vs. rotor position are shown in Fig. 4 and Fig. 5, respectively. By comparing Fig. 2 with Fig. 4, we can observe that the analytical method is conservative. The calculated total

weight of the motor is about 11.8 lbs, which is very close to that of the preliminary design. The efficiency of the SRM is 75%, and it has been found that 82% of the power loss is due to copper loss. In the future, high-flux-density lamination materials, such as permendur, will be investigated to improve the SRM efficiency and optimize the SRM design.

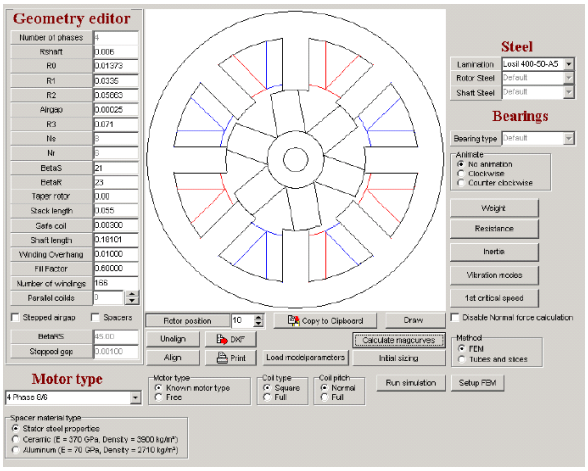


Fig. 3. SRM design interface in SRDaS.

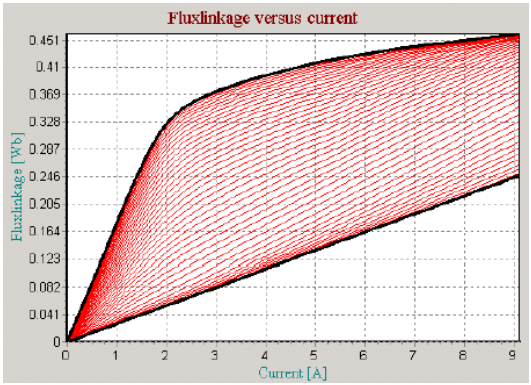


Fig. 4. Flux linkage vs. current in SRDaS simulation.

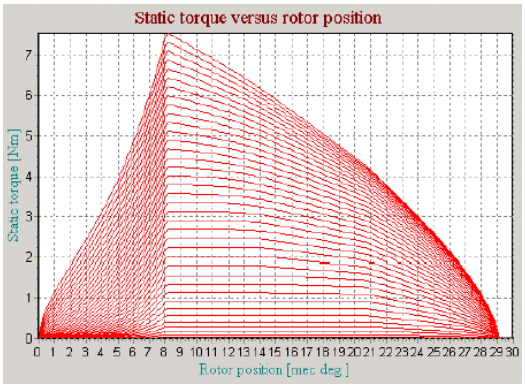


Fig. 5. Static torque vs. rotor position (as functions of current).

III. SENSORLESS CONTROLLER DESIGN

For the converter stage, the classic bridge converter is selected as being suitable, as its fault-tolerance capability is very important for the LCAC application. Fig. 6 illustrates the topology of the power converter, in which the coils A, B, C & D are the "phases" of the SRM.

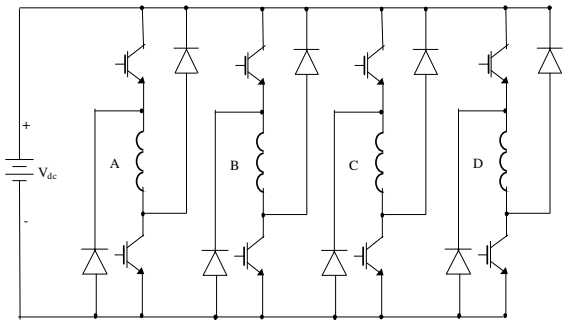


Fig. 6. Classic bridge converter.

The excitation of the SR motor phase current needs precise control with respect to its rotor angle. The phase inductance variation is the main challenge for the controller design, but it also makes it possible to realize the sensorless control just based on the magnetic characteristics of the SR motor.

One approach [7] is to build a 3-D look-up table of the rotor angle, phase current and the flux, which can be obtained through FEM analysis or the experimental results. The flux could be obtained by voltage integration. Based on the current and the calculated flux, the instantaneous rotor position can be found from the look-up table. Unfortunately the integration step makes this method unsuitable for low speed operation, especially during the starting period. Since this application focuses on frequent low-speed, high torque ranges, pulse voltage and current waveform detection is a better choice.

Another current-changing-ratio method is mentioned in [8]. Following the equation:

$$\Omega^T(\theta_{t1})\left[I\left.\frac{d\Lambda(i_k)}{di_k}\right|_I+\Lambda(I)\right]=\frac{(1-\alpha)V}{\Delta i}\left[\frac{1}{t_{on}}+\frac{1}{t_{off}}\right]^{-1}$$

Where,

$\Omega(\theta_{t_1})$ --Position matrix at rotor angle θ_{t1}

I -- Average current

$\Lambda(I)$ -- Phase inductance profile matrix for aligned, midway, and unaligned positions
Δi -- Peak-peak hysteresis current band
α -- -1 for hard chopping, 0 for soft chopping
V -- DC link voltage
t_{on}, t_{off} -- Rise and fall time in one cycle

By analyzing the real phase current in its constant range, we can easily estimate the rotor speed, and no continuous voltage pulse is necessary. Most importantly the variation of the back emf and the phase resistance will have no influence on the calculation. The preciseness of the total system will mainly be determined by the current sensor and the system timer. In fact this method needs some information from the analytical SRM model. It is somewhat similar to the flux-current-angle method. Since the hysteresis current band is always set by the control, and the phase current is sufficient to determine the inductance portion, which can be realized by a look-up table, the speed estimation is very fast. The motor speed is locked by a digital phase-locked loop (DPLL) [9], which filters the unexpected noise. With occasional initial angle checked by the voltage pulse strategy, high performance sensorless position control is developed.

IV. PROOF-OF-CONCEPT DEMONSTRATION

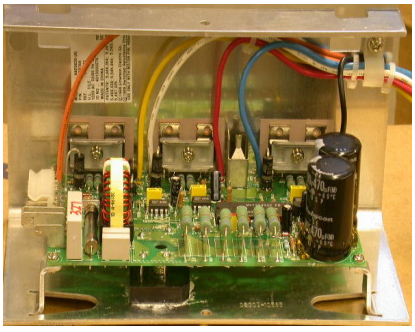
A proof-of-concept demonstration has been developed to show the basic functionality of the proposed SRM-based actuator, as shown in Fig. 7. Fig. 7 (a) shows the actuator system raising a weight as a demonstration of linear thrust capability. A four-start ball screw (1 inch in diameter, 1 inch pitch) is used in this proof-of-concept configuration. Fig. 7 (b) shows the power converter.

A maximum weight of 33.5kg (74.4lbs) has been successfully lifted with the setup shown in Fig. 7 (a), proving the proper operation of the entire actuator system. Note that the low operating thrust, compared to the required thrust, is due to the low mechanical advantage of the ball screw (only 2.5) and the limited torque capability of the proof-of-concept SRM system. In the final product, a high efficiency (≥ 0.9) roller-screw with higher mechanical advantage, along with a fully scaled SRM, will enable the full operating thrust.

V. CONCLUSIONS AND FUTURE WORK

This digest proposed a switched reluctance motor (SRM) based actuator for use on the landing craft air cushion (LCAC), to replace the existing hydraulic systems that control the steering vanes. The proposed SRM-based actuator is intended to enable the reduction of complexity, weight, and maintenance associated with conventional hydraulic systems. The proposed actuator consists of an SRM and a high-efficiency roller-screw with suitable mechanical advantage. A preliminary SRM has been designed using an analytical method, and then verified with SRDaS. A proof-of-concept demonstration has been developed to show the basic functionality of the proposed SRM-based actuator. Future work includes investigating the application of high-flux-density lamination materials to optimize the SRM design, as well as optimizing speeds and dimensions. Experimental results for the fully scaled actuator will also be included in the final paper.

(a) Raising a weight



(b) Power converter
Fig. 7. Proof-of-concept demonstration.

ACKNOWLEDGEMENT

This work is sponsored by the Office of Naval Research (ONR) Small Business Technology Transfer Program (STTR), under contract # N00014-03-M-0312. Special thanks also to Emerson for providing the SRM and converter.

REFERENCES

[1] Robert E. Leonard and Thomas B. Dade, "The All Electric Ship: Enabling Revolutionary Changes in Naval Warfare," https://aeps.onr.navy.mil/techpapr.nsf/0/0dd7527e8a8206ff85256 c50052a697/$FILE/AllElectricShip.PDF.

[2] http://www.pml.tno.nl/en/pt/downloads/all_electric_ship.pdf

[3] http://www.marinetalk.com/articles_HTML/ SAT009104013TU.html.

[4] R. Krishnan, Switched Reluctance Motor Drives: Modeling, Simulation, Analysis, Design, and Applications, CRC Press, Boca Raton, 2001.

[5] P. Vijayraghavan, "Design of Switched Reluctance Motors and Development of a Universal Controller for Switched Reluctance and Permanent Magnet Brushless DC Motor Drives," Ph.D. Dissertation, Virginia Polytechnic Institute and State University, 2001.

[6] P. O. Rasmussen, "Design and Advanced Control of Switched Reluctance Motors," Ph.D. Dissertation, Aalborg University, 2002.

[7] R. B. Inderka and R.W.A.A. De Doncker, "DITC-Direct Instantaneous Torque Control of Switched Reluctance Drives," *IEEE Trans. on Industry Applications*, vol. 39, Issue 4, July-Aug.2003, pp. 1046 –1051.

[8] F.R.Salmasi, B.Fahimi, H.Gao, and M. Ehsani, "Robust Sensorless Rotor Position Detection in Switched Reluctance Motor for Low Speed Applications," PESC 2001, vol. 2, pp. 17-21.

[9] T. Wakasa, Hai-Jao Guo, and O. Ichinokura, "A Simple Position Sensorless Driving System of SRM Based on New Digital PLL Technique," *IECON 02*, IEEE 28th Annual, vol. 1, pp. 502 –507.